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A 40 GHz CMOS Transceiver for

The Customer Premise Equipment Unit

Of a Radio-over-Fiber System

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*Abstract*—A miniature 40 GHz transceiver designed using a 0.13-µm RF CMOS process is presented in this paper. The transceiver employs a direct-conversion architecture. A phase-locked-loop (PLL) and supporting digital circuits however, are not included. The receiver shows a power gain of about 35 dB, whereas the transmitter achieves a power gain of about 32 dB.

*Index Terms*—Customer premise equipment (CPE), RF CMOS, Radio-over-fiber (ROF), Transceiver.

# INTRODUCTION

T

HE recent explosion of high-data rate fixed and mobile wireless communications has put into focus the future need for low-cost and miniature fully integrated systems that enable the transfer of gigabits-per-second data reliably over a certain distance [1]. The exploitation of mm-wave frequencies for high data rate transfer is a natural step due to the immense bandwidths made available for commercial use either freely or relatively low-cost [2]. One of the possible applications for mm-wave and wideband communications is radio-over-fiber (RoF), which seamlessly integrates optical and wireless communications by minimizing intermediate equipment or devices by modulating an optical carrier using an RF signal [3]. However, one of the biggest obstacles to the widespread commercialization of RoF is the cost of the optical and wireless components. The cost of the remote antenna unit (RAU) and customer premise equipment (CPE) can be minimized by fabricating the transceivers using silicon CMOS technology.

In this paper, we present a miniature Q-band transceiver designed using a low-cost 0.13-µm RF CMOS process for use in a 40 GHz radio-over-fiber communications system (Fig.1). To date, there have been no literature on 40 GHz CMOS transceivers for RoF applications, although Q-band CMOS devices have been reported [4]-[7]. The transceiver uses a direct conversion architecture, thus minimizing the number of components on-chip.

# Device Characteristic And CMOS Process

The Q-band transceiver is designed and simulated using Silterra's 0.13-µm RF CMOS process. This process has 1 poly and 8 copper metal layers for interconnections as well as passive devices. The top metal is 3.3-µm thick to minimize passive losses. The process uses deep n-well as well as 1fF/µm2 MIM capacitors. The *f*t of the process is 81 GHz, and the silicon substrate resistivity is 10 Ω.cm.

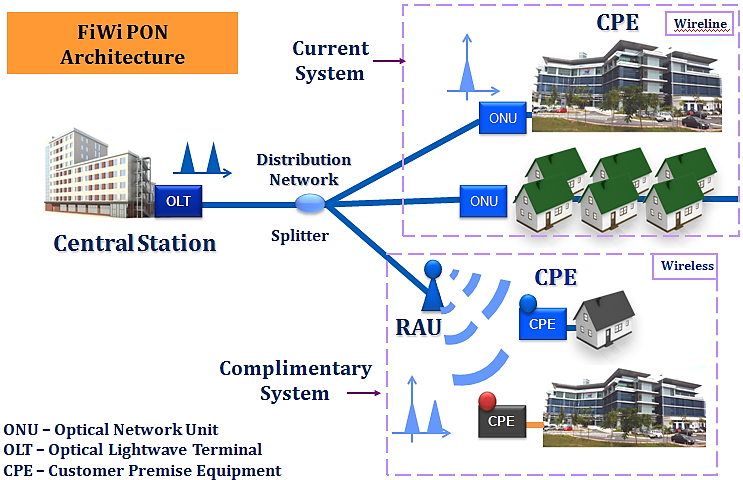


Fig. 1. A typical application for RoF. The CPE will be used in the mobile or stationary equipment in houses. Parts of the transceiver will also be used in the RAU.

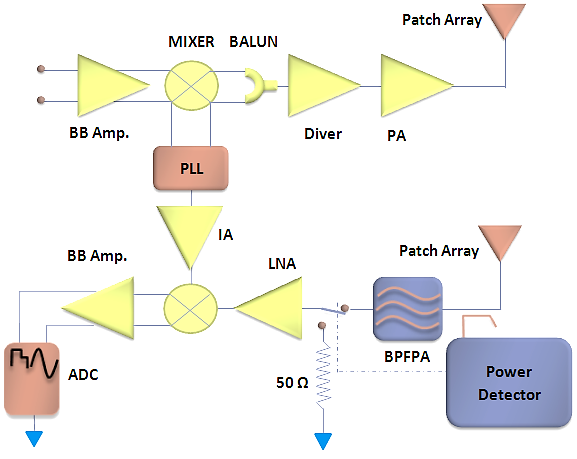


Fig. 2. The transceiver block diagram to be used in the CPE of the RoF system.

# Circuit Design

The architecture used for the transceiver is direct conversion. DC wandering due to direct conversion is solved by using compensation circuits not covered in this paper. Fig. 2 shows the transceiver parts designed and simulated in this work. The frequency range for the transmitter is between 37 to 40 GHz, and for the receiver is between 40 to 42.5 GHz.

## Receiver

The receiver is single-ended input, and differential output. The LNA architecture is a 3-stage, common source architecture as shown in Fig. 3. Silterra models were used for all the passive devices. In addition, no transmission lines were used in order to minimize the total size of the chip.

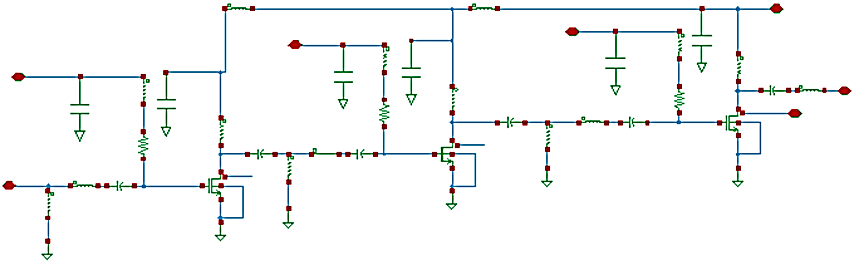


Fig. 3. Schematic for the 3-stage common-source 41.5 GHz LNA

The mixer (Fig. 4) uses a previously used quadrature architecture with broadband baseband matching [8]. A hybrid coupler is used to provide the necessary quadrature inputs to the active devices, thus producing 180-degree out-of-phase outputs to be fed to the baseband amplifier. Broadband output matching is optimized to a certain impedance in order to provide maximum signal transfer to the baseband amplifier throughout the entire signal bandwidth (Fig. 5).

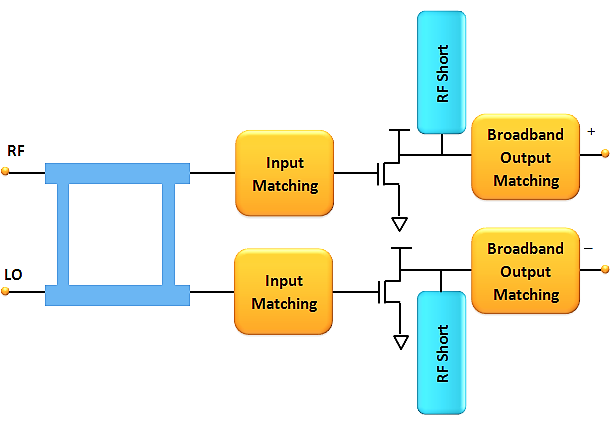


Fig. 4. Block diagram for the down-conversion mixer.

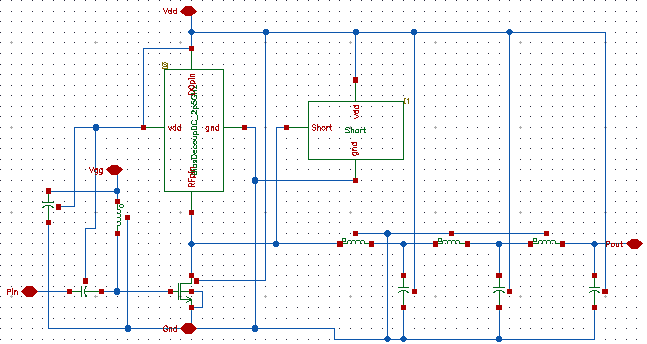


Fig. 5. Schematic for output stage of the quadrature mixer.

The baseband amplifier has a differential input, differential output configuration. The gain is also fixed, but may be replaced by a variable-gain version presented in the transmitter section.

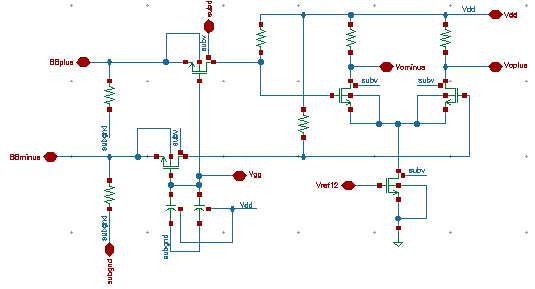


Fig. 6. Schematic for the receiver baseband amplifier

The injection amplifier (IA) is a two-stage, common-source amplifier for the purpose of amplifying the output of the phase-locked loop (PLL) and for RF/LO Isolation. Amplification is needed as the output of the PLL might not be able to provide enough power to drive the mixer LO input.

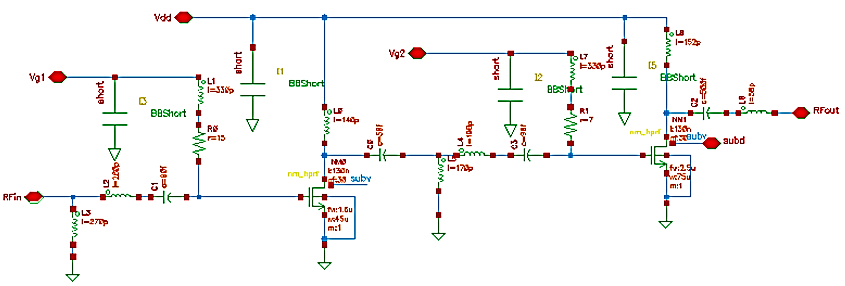


Fig. 7. Schematic for the injection amplifier (IA).

Fig. 8 shows the simulation setup for the complete receiver.

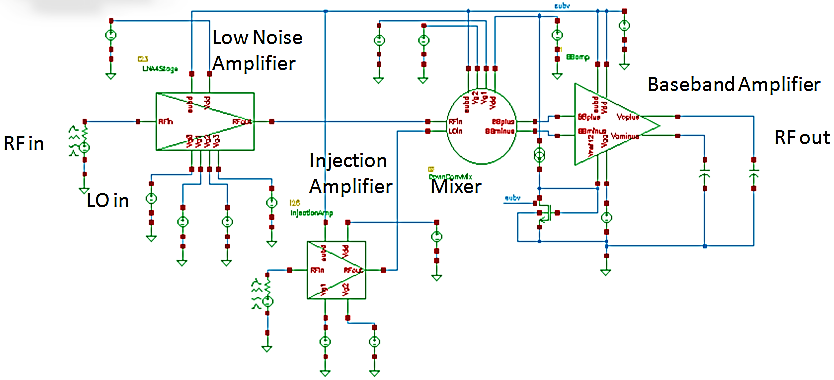


Fig. 8. Simulation setup for the entire receiver chain.

## Transmitter

The transmitter also uses a direct conversion architecture. Differential architecture is used from the baseband amplifier up to the mixer, where a lumped BALUN will convert the mixer output to single ended for subsequent amplification.

The baseband amplifier has a variable-gain architecture. Standard current-steering, level shifter, and buffer circuits are used (Fig. 9).

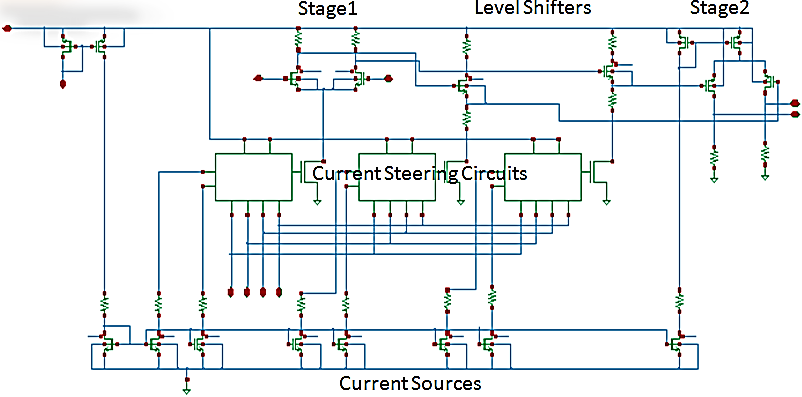


Fig. 9. Schematic for the variable-gain baseband amplifier

The up-conversion mixer uses a Gilbert-cell architecture since isolation is no longer such an important requirement (Fig. 10). A 3V DC supply provides the headroom needed to maintain correct biasing for the stacked transistors used in the mixer.

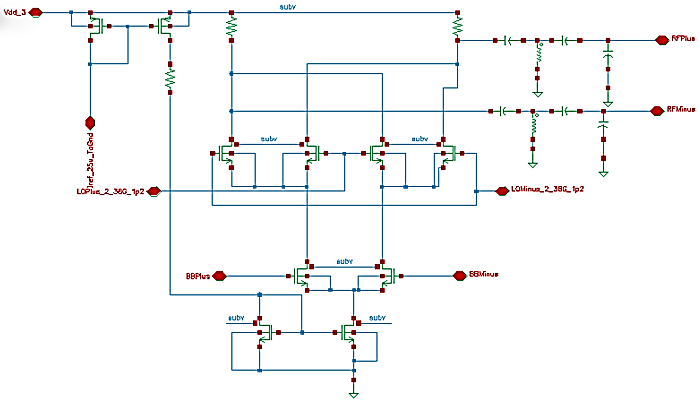


Fig. 10. Schematic for the Gilbert-cell mixer for up-conversion

The driver amplifier (DA) for the power amplifier (PA) consists of a 4-stage common-source architecture. The PA consists of a 2-stage common source amplifier, though the 2nd stage consists of 3 common source amplifiers in parallel. The output power of the 2nd stage amplifiers are combined using a Wilkinson power combiner. Fig. 11 and Fig. 12 shows the driver as well as power amplifier implementation.

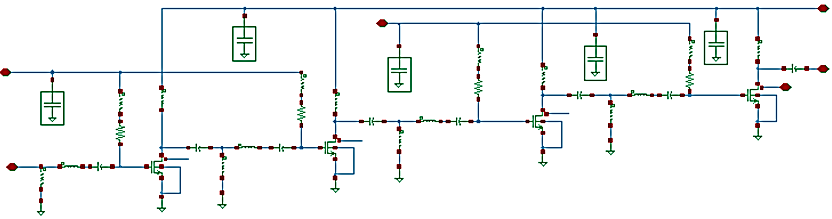


Fig. 11. Schematic for the driver amplifier.

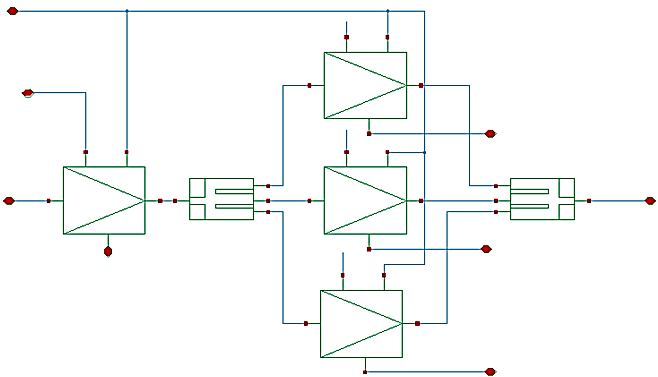


Fig. 12. Schematic for the power amplifier.

The setup for the entire transmitter for simulation is shown in Fig. 13.

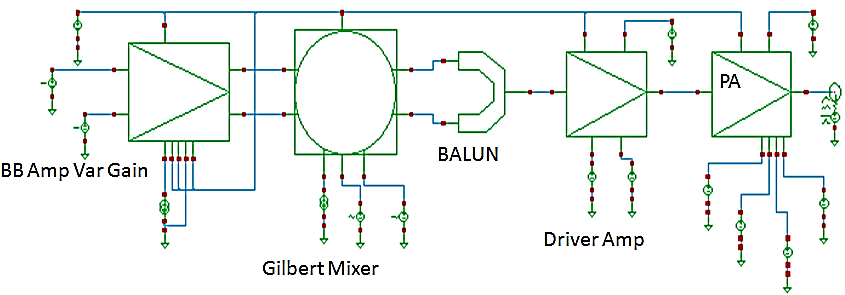


Fig. 13. Setup for the transmitter simulation.

# Simulation Results

## Receiver

The receiver was simulated with variable input power (from -65 to -25 dBm) under two different conditions, low baseband frequency (50 MHz) and high baseband frequency (1.5 GHz). Fig. 14 and 15 show that the baseband amplifier compresses quicker at low frequency whereas at high frequency, the low-noise amplifier compresses quicker. In general, the receiver achieves a power gain (assuming output voltage is converted to power using 50 Ω load) of around 35 dB.

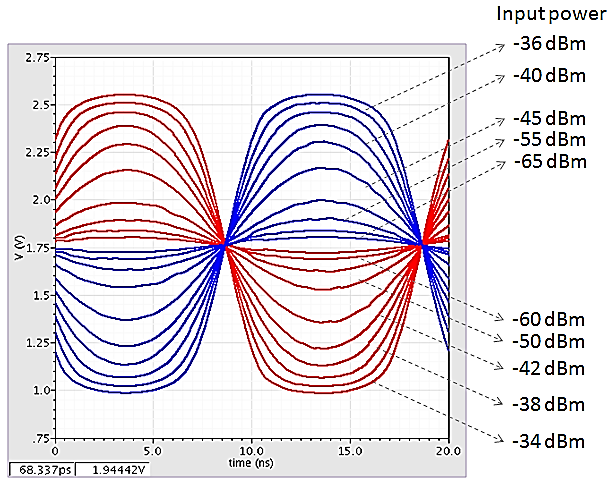


Fig. 13. Simulated output waveforms for Transmitter at

Low Baseband Frequency of 50 MHz

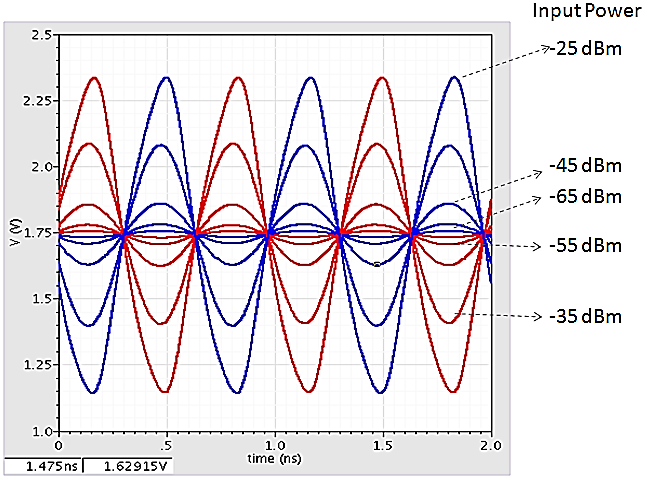


Fig. 14. Simulated output waveforms for Transmitter at

High Baseband Frequency of 1.5 GHz

## Transmitter

The simulations for the variable-gain amplifier is shown in Fig. 15. A gain range of more than 10 dB is achieved for a 4-bit control input.

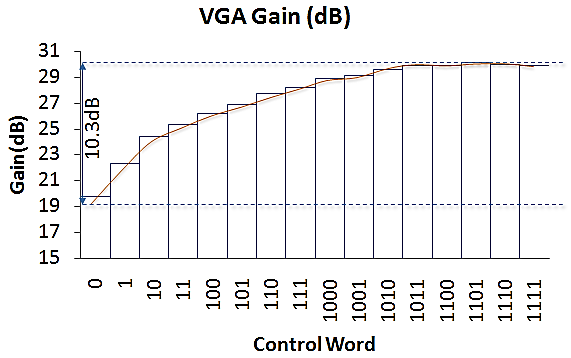


Fig. 15. Simulated gain for the variable-gain baseband amplifier.

The local oscillator signal power is set to 1.2 dBm @ 38 GHz whereas the voltage input to the variable-gain baseband amplifier is 20 mV peak-to-peak @ 1.5 GHz. Fig. 16 and Fig. 17 show the harmonic balance simulations.

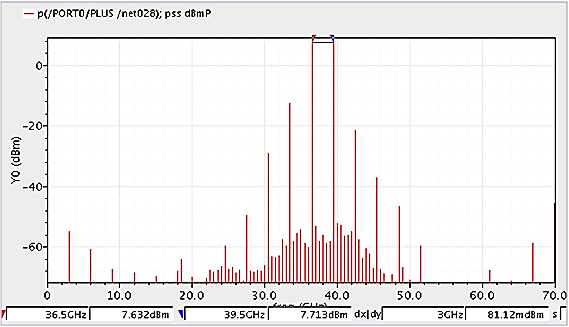


Fig. 16. Simulated output power for the two sidebands (36.5 and 39.5 GHz).

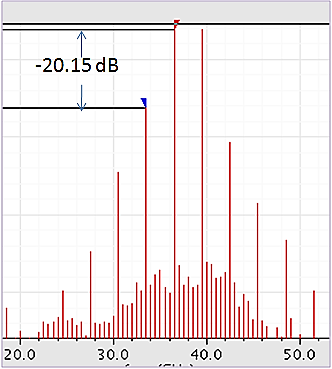


Fig. 17. Simulated output power of the non-linear components of the transmitter.

The simulated transmitter produces an output power of around 7.7 dBm. Assuming that the baseband amplifier has an input match of 50 Ω and an input power of -24 dBm (20 mV p-p), the power gain of the transmitter is around 32 dB. The closest third-order frequency component is more than 20 dB lower than the carrier.

# Conclusion

## This work shows the possibility of using a low-cost 130- nm silicon CMOS process for fabricating parts of a 40 GHz radio-over-fiber system. Future research needs to be done on improving the uniformity of the gain for the wideband signal frequencies. In addition, DC offset due to self-mixing may be minimized even more by implementing an injection or RF filter.

Acknowledgment

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