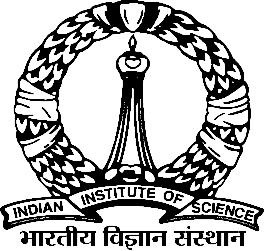
**Anurag Nigam**

Goal: Technology Acquisition, Practice & Dissemination

M.Tech in Satellite Technology & Applications

Indian Institute of Science (IISc.), Bangalore, Year 2000

13 Years of Industry Experience and 1 year of Teaching Experience

2 Years of Research Experience

**Career Highlights**

M.Tech

in Satellite Technology & Applications, IISc

RFIC Designer

IBM, Boston,

MA USA

US Patent

US 7165200 B2

*Signal Path using Sub-Chip Sampler*

Founded NatTel Microsystems Pvt. Ltd.

Adopted Teaching Career

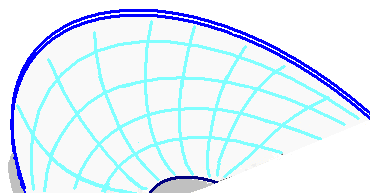
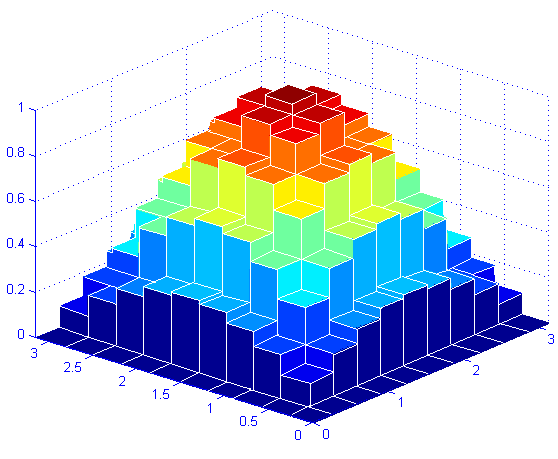
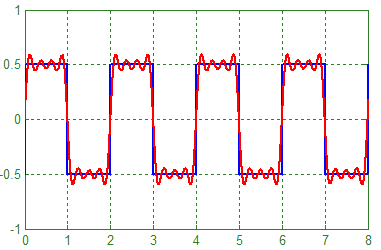


**25 March, 2000**

**24 Feb., 2000**



**16 Jan., 2007**



**18 Dec., 2007**



**3 Aug., 2015**



**Other Career Moves**



Registered PhD in

Electrical and Computer Engineering Department, 2003 to 2004



Registered PhD in

Supercomputing Education Research Center, IISc, 2004

Could not finish due to financial liabilities

**Experience in Chronological Order**

Assistant Professor,

Aug. 3, 2015 to present

Dec., 2007 to June, 2015

May, 2006 to Dec., 2007

Jan., 2005 to March, 2006

Feb., 2000 to Oct., 2002

Deogiri Institute of Engineering and Management Studies, Aurangabad

Director,

NatTel Microsystems Pvt. Ltd., Goa

Assistant Technical Manager,

Persistent Systems Ltd., Goa

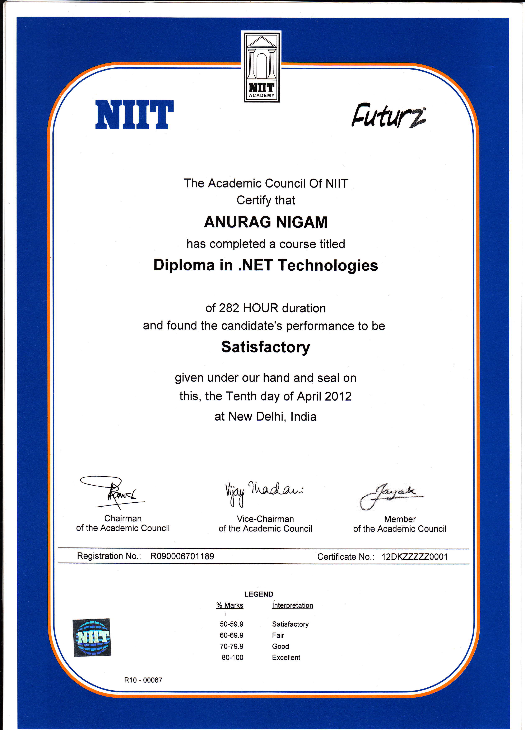
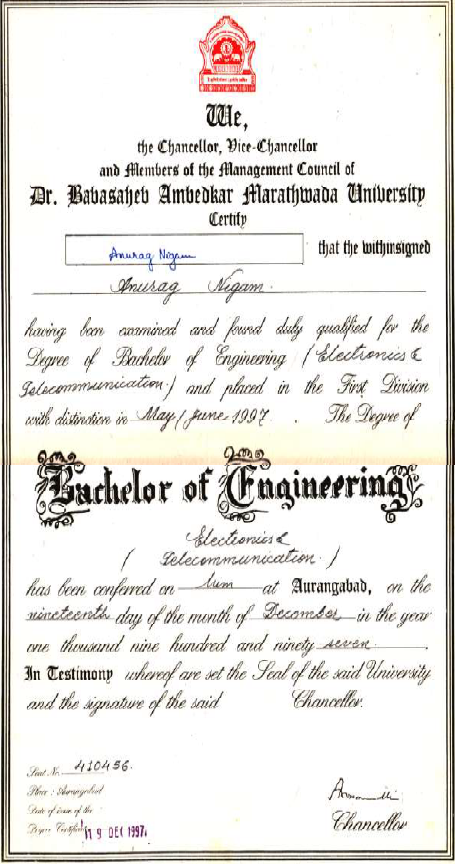
Technical Manager,

RF Arrays Pvt. Ltd., Nagpur

RFIC Designer,

IBM Microelectronics, MA, USA

**Education**

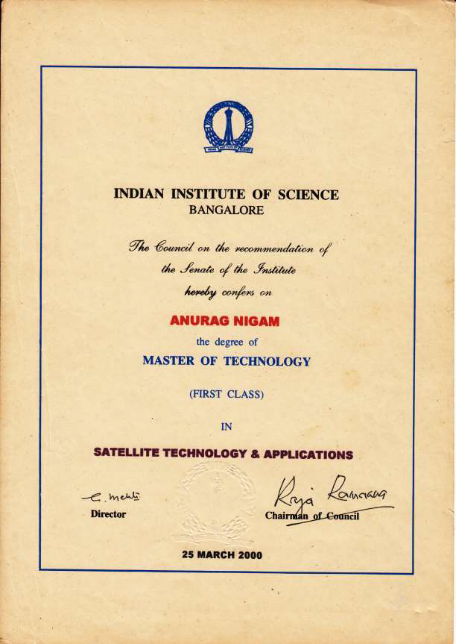


**Master of Technology**: *Satellite Technology and Applications (Year 2000)*

**Institute:** *Indian Institute of Science, Bangalore*

**Specialization:** *Microwave Integrated Circuits in C and X Band*

**CGPA:** ***6.9/8.0 First Class Rank II***



**Bachelor of Engineering**: *Electronics and Telecommunications (Year 1997)*

**Institute:** *Jawaharlal Nehru College of Engineering*

**Specialization:** *Processing for Artificial Intelligence, Expert Systems*

**Aggregate %: *76% First Class with Distinction, Silver Medalist***

**Diploma:** *Microsoft .NET Technologies (Year 2012)*

**Institute:** *NIIT, New Delhi*

**Skillset**



**Semiconductor Processes used**



**MMIC, RFIC, mm Wave IC Component Design and Layout**

Radio Front-End (LNA, PA, Switch),

VCO, Mixer, Fractional N PLL,

Microstrip Patch Antenna,

Microwave Filters,

Integrated Phase Shifter,

Digital Attenuator,

Direct Conversion Transceiver

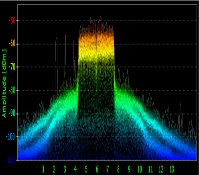
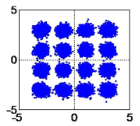
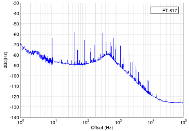
**RF Measurements**

PA Measurements-Gain Compression,

ACPR, EVM, Load Pull

LNA Measurements- Noise Figure

VCO Measurements- Phase Noise



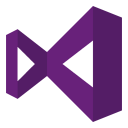
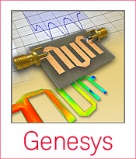
**Equipment used**

VNA, Spectrum Analyzer, Power Meter, Power Sensor, Noise Figure Meter, Maury Bench, Cascade Probe

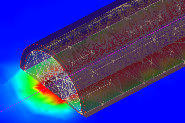
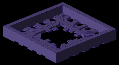
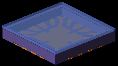
**Software used**



**ADS**



**Packaging & EM Sim**



**US Patent & Publication**

*System and method for characterizing a signal path using a sub-chip sampler,* US 7165200 B2

*“SiGe Power Amplifier ICs with SWR Protection for Handset Applications*”, Philip Antognetti, David Helms, Anurag Nigam, James Griffiths, Kenneth Louie and Mark Doherty, IBM Boston RFIC Design Center, IEEE Microwave Journal, June 2001

*“A 40 GHz CMOS Transceiver and Radio Front-End for the Customer Premise Equipment Unit of a Radio-over-Fiber System”,* Nazif E. Farid et al. (Telekom Research & Development Sdn. Bhd., Malaysia), Anurag Nigam (NatTel Microsystem Pvt. Ltd., India), IEEE International Conference on Ultra Wideband, 2013

**List of Projects Completed**

1. SiGe WCDMA PA (Freq. 1.92-1.98 GHz, 39% PAE, -39dBc ACPR, 24dBm Pout, 24dB Gain, with on chip Band gap bias circuit)
2. GaAs MESFET Class E PA (Freq. 5 GHz, 69% PAE, 76% Drain Efficiency, 28dBm Pout, 10 dB Gain)
3. GaAs MESFET Class E PA (Freq. 10 GHz, 58% PAE, 63% Drain Efficiency, 28 dBm Pout, 10 dB Gain)
4. Flip Chip IS95 PA (42% PAE, -45dBc ACPR, 28dBm Pout, 29dB Gain, with on chip Band gap bias circuit)
5. InGaAs p-HEMT 802.11 b/g PA (Freq. 2.4-2.5 GHz, 16/19 dBm Pout, EVM 3.8%, 28.4 dB Gain, 80/110 mA total current)
6. SiGe Mixer (RF Freq. 61.8-63.5 GHz, LO Freq. 57 GHz), Single-ended input Differential output, Conversion Gain -1 dB, total current 12 mA, DC 3.3 V/1.8V, Gain Balance < 0.3 dB, phase balance < 2.8 degrees)
7. SiGe LNA (Freq. 61.8-63.5 GHz), NF 7.23 dB, Gain 8 dB, Quiescent Current 17 mA, DC 3.3 V
8. SiGe VCO (2.6-2.9 GHz, 2.9-4.5V DC Supply, 7.74mW Pout, -131dBc/Hz @10MHz offset Phase Noise, 8kHz/°C Thermal Stability, with on chip bias circuit)
9. SiGe Dual Modulus Fractional N PLL @ 400 MHz
10. SiGe Large Dynamic Range Gilbert Cell Mixer down-converter @ 2.8 GHz
11. SiGe Quadrature Mixer @ 60 GHz
12. SiGe LNA @ 60 GHz
13. Dual Band Fractional N PLL for Wi-Fi @ WiMAX bands in 0.13 um Silterra CMOS Process.
14. 189 W, 200 to 260 MHz, 46%DE, Band Power Amplifier for Radar Applications using Freescale Power LDMOS
15. 150 W, 60 to 105 MHz Band Power Amplifier Design using Freescale Power LDMOS
16. X-band Radar Core Design- in TRIQUINT PHEMT Process
17. 9.6 W -1dB Compression Point, 9.4 to 10.4 GHz, 17 dB Gain, 42% DE, PA Design
18. 0-360-degree Phase Shifter Design, 9.4 to 10.4 GHz
19. 6 Bit Digital Attenuator with 0.5 dB step
20. 3.8 dB NF,9.4 to 10.4 GHz 16 dB LNA
21. Ka-Band LNA Design – in UMS 0.15 um PHEMT Process, 9 dB Gain, 34.5 to 35.5 GHz, 1.8 dB NF, 5 dB input at 1 dB Gain Compression
22. Ka-Band PA Design – in UMS 0.15 um PHMT Process, 16 dB Gain, 34.5 to 35.5 GHz, PAE 37%, P1dB 30 dBm
23. 37.5-39.5 GHz (Receiver) 40-42 GHz (Transmitter) for Last Mile Connectivity for Fiber to Home Connectivity, Direct Conversion CMOS Transceiver.
24. SiGe NADC/ PDC PA (PAE 52%)
25. InGaAs p-HEMT 802.11 b/g/BT FEM (Freq. 2.4-2.5 GHz, LNA + PA + SPTT + Logic Decoder + all matching on-chip, 1.4mm x 1.4mm die size fits in 3mm x 3mm QFN)
26. InGaAs p-HEMT 802.11 a FEM (Freq. 4.9-5.95 GHz, LNA + PA + SPTT + Logic Decoder + all matching on-chip, 1.4mm x 1.4mm die size fits in 3mm x 3mm QFN)

**List of Teaching Programs & Workshops conducted**

\*Advanced Design System is Electronic (IC) Design Software

1. One Day “Antenna Design” Training, Medium: Adobe Flash, Agilent, Singapore
2. One Day “MMIC Design” Training, Medium: Power Point, SAMEER, Kolkata
3. Two Days “Power Amplifier Design” Workshop, Space Application Center, ISRO, Ahmedabad
4. Visiting Lecturer, Birla Institute of Technology, Pilani-Goa Campus, Goa
5. Five days “SiGe BiCMOS Design” Training, R&D Telecom Malaysia
6. One Month “Millimeter Wave LNA & VCO Design” Workshop, R&D Telecom Malaysia
7. One Month “Dual Band (Wi-Fi/WiMAX) PLL Design for Direct Conversion Transceiver” Workshop, R&D Telecom Malaysia
8. Three Days “Advanced RF Design using Genesys” Training, MACRES, Malaysia
9. Three Days “Advanced Communication System Design using Ptolemy” Training, University of Malaysia, Kuala Perlis, Malaysia
10. Five Days “Advanced RF Design using ADS” Training, Motorola, Penang, Malaysia
11. Two Day Training, “Advanced Design System\*”, Baba Ramdev College of Engineering, Nagpur
12. Three Day Training, “Advanced Design System”, Ambedkar Institute of Technology, New Delhi
13. One Day Training, “Advanced Design System”, Velamal Engineering College, Tamil Nadu
14. Two Day Training, “Advanced Design System”, PSG College of Technology, Coimbatore
15. One Day Training, “Advanced Design System”, MCET, Coimbatore
16. Two Day Training, “Advanced Design System”, VIT, Mumbai
17. Five Day Training Workshop, “Linear Circuit, Simulation & Synthesis using Genesys”, Agilent Technologies, Germany

**References**

Mark Doherty, VP Skyworks, Tel. 001(978)589-9959

Dr. Nitin Jain, CTO, Anokiwave Inc., nitin@anokiwave.com