Introduction

This Workshop is designed to provide in-depth knowledge of HBT and Circuits. We provide detailed discussions on Voltage and Current References, Radio Front-End Circuits, Transceiver Circuits and High Speed Logic Circuits. We cover in detail high frequency layout issues in SiGe RFIC and MMIC Circuits from thermal, noise and parasitic standpoint.

Structure of Workshop

The workshop is designed for five days. The workshop is organized into chapters. Each chapter begins with a tutorial on the central theme of the chapter. The tutorial demonstrates through simulation covers various concepts and the underlying theory. Tutorial is followed by hands-on exercise in ADS for the students to get comfortable with the concepts and try some of their ideas. Healthy discussion is encouraged to address curiosities and clear doubts.

Contents of the workshop

Day1

1) Introduction to Semiconductor Material Properties and Technologies
    a. Bandgaps and Lattice Constants
    b. Velocity Overshoot
    c. Bandgap Discontinuity and Narrowing
    d. Strained Semiconductors and Critical Thicknesses
    e. Electron and Hole Mobility
2) HBT DC Performance
    a. Early Voltage
    b. Emitter Crowding
    c. High Injection Barrier Effects
    d. Current Gain and Early Voltage Product
    e. Temperature Dependency of Forward Current Gain in HBTs
    f. Current Gain Roll-off in Graded Base HBTs
    g. Self Heating Effects
3) HBT RF Performance and Transient Performance
    a. Output Capacitance
    b. Transconductance
    c. Heterojunction Capacitance
    d. Base Transit Time and Cut-off Frequency
    e. Maximum Frequency of Oscillation
    f. Collector-up Vs Emitter-up HBT Performance

g. Noise
h. S-Parameters

4) HBT Device Structure
   a. Abrupt and Graded Heterojunctions
   b. Setback Layers
   c. Graded Base HBTs
5) Breakdown and Thermal Instability
   a. Reverse Base Current Phenomenon
   b. Avalanche Effects
   c. Emitter Collapse in HBTs
6) Design for Thermal Stability
   a. Emitter and Base Ballasting
   b. Emitter Thermal Shunt
7) Reliability and Yield Issues
   a. Thermal and Electrical Overstress Issues in Circuits

Exercise1

Study Characteristics of PN-Junction Diodes and their dependency on process parameters and bias point.

Exercise2

Study DC and Breakdown Characteristics SiGe HBT when biased with forced current and forced voltage at the base.

Day2

8) Biasing HBT and BiCMOS Circuits for Across Temperature Performance
   a. Simple, Cascade and Cascode Current Mirrors using HBTs
9) PTAT Current References using HBTs
10) Startup Circuits and Frequency Compensation
11) CTAT Voltage References
12) Temperature Independent Current References
13) PTAT Square Current References using HBTs

Exercise3, 4, 5, 6, 7

Design various forms of current mirror and compare their performance- PMOS, NMOS, BJT, Cascode and Wide Swing Cascode Current Mirrors

Exercise8, 9, 10

Design PTAT Current Source, CTAT Voltage Reference and Band Gap Voltage Reference

Day3

14) Microwave and RF Components
    a. Maxwell's Equations, Constitutive Relations, Transverse Electromagnetic Waves, Propagation in Space
    b. Transmission Lines- Microstrip Lines & Coplanar Waveguides, Dielectric and Conductor Losses, TEM Propagation, Design Trade-offs.
    c. Coaxial-to-CPWG Transition Design
15) Network Parameters- S, Z, Y, ABCD, their conversion and application to passive modeling.
16) Microwave Passives- Stacked Inductors, MIM Capacitors, Broadband Spice Modeling
17) Bias Decoupling Circuits using lumped and distributed passives
18) Single pole matching using lumped components, matching using Microstrip components, broadband matching techniques.

Exercise11
Design 50 Ohm Microstrip Line and Coplanar Waveguide

Exercise12
Design Matching Networks using lumped components and distributed components, design broadband matching networks

Exercise13
Design Stacked Inductors and MIM Capacitors and fit broadband SPICE Models for use in circuit simulations

Exercise14
Design bias decoupling circuits using lumped components, design high Q bias decoupling circuits using stubs, design broadband bias decoupling circuits using radial stubs and design multi-band bias decoupling circuits.

Day4

19) Power Amplifiers in TDD and FDD Systems, their performance criteria, Classes of Power Amplifiers and their comparison, concept of linearity and back-offs for linear power amplifiers

20) Characteristics of Power Amplifiers- Gain, PAE, Return Losses, Stability, Linearity (ACPR and %EVM), Inter-modulation distortion, AM-AM and AM-PM Conversions
21) High Efficiency Class E Amplifier Design and Operating Principles
22) Concept of Load-Pull
23) Self-heating in HBTs, Thermal Instabilities, Layout that is thermally optimum for HBTs, Emitter Collapse in SiGe HBTs, Emitter and Base Ballasting
24) Losses in a Power Device

Exercise15

Design Class E Power Amplifier in X and Ku Band

Exercise16

Small Signal Design of a Gain Stage, Low Noise Amplifier Design, Concept of Noise Figure and its dependency on device and circuit topologies.

Exercise17

Design Large Signal Amplifier assuring across frequency, across power, across supply voltage performance and stability.

Exercise18

Perform Single Tone and Two Tone Simulations on a Power Amplifier.

Exercise19

Optimize Power Amplifier for PAE using Load-pull in ADS

Day5

25) RFIC Circuit Example- VCO Design, Concept of phase noise, Using Symmetry of Waveform to ensure low phase noise in poor 1/f noise devices, Concept of perturbation and use of Tail Capacitor to minimize Phase Noise
26) Transient Simulation of VCO to study start-up characteristics
27) Phase Noise Simulations using differential oscillator port
28) RFIC Circuit Example- High Input Dynamic Range Mixer Design, BALUN Design, Large Signal Simulations of a Mixer.

Exercise20, 21, 22

Design circuit components of a differential VCO Core

Exercise23

FET Gilbert Cell Mixer Design optimized of large input dynamic range.