MMIC & MIC Design Flow of Linear & Saturated Power Amplifiers using Agilent Advanced Design System

Anurag Nigam, *CEO*, NatTel Microsystems Pvt. Ltd., Anurag Bhargava, *Application Engineer*, Agilent Technologies India Pvt. Ltd.

***Abstract*- This paper discusses MMIC and MIC Design Flow that guarantees first-pass success of Power Amplifier Design using Agilent Advanced Design System Software. The case study involves design of a saturated power amplifier operating in C band and a linear power amplifier operating in S band. Industry examples are presented to validate the design flow.**

***Index Terms*- MMIC (Monolithic Microwave Integrated Circuit), MIC (Microwave Integrated Circuit), PA (Power Amplifier), PAE (Power Added Efficiency), ACPR (Adjacent Channel Power Ratio), %EVM (Percentage Error Vector Magnitude), EM (Electro-Magnetic) Simulations**

I. Introduction

Spectrum costs to service providers in Licensed Frequency Band. This has resulted in numerous modulation schemes that efficiently utilize frequency band. In few applications, performance reliability of data link is important. In wireless systems, modulated carrier has to be boosted in power at the transmitter side before transmission. This is to guarantee certain Signal to Noise Ratio at the receiver. Power Amplifier (PA) is power gain block just before antenna that boosts the transmitted power.

Power Amplifiers operating in Microwave Frequency Band (300 MHz to 300 GHz) are designed with components either fabricated on same wafer (called MMIC PAs) or assembled on printed circuit board (called MIC PAs). This paper discusses design flow for both kinds of PAs. Section II discusses operation of a typical PA and explains various performance criteria from industry stand point. Section III presents briefly a design flow typically followed in industry.

Section IV discusses operation of a typical high efficiency saturated PA (called Class E) followed by circuit topology and design equations. This section also presents discussion for a linear power amplifier on similar lines.

Section V demonstrates techniques to design and model passive components. This discussion proves that EM Simulators are indispensable for Passive Component and Evaluation Board Design and Verification.

Section VI discusses Small Signal Simulations like S-Parameter and Large Signal Simulations like Harmonic Balance and Envelope, applicable to Power Amplifier Development. This section discusses stability issues of a multistage PA and techniques to optimize performance using simulations.

Section VII demonstrates generation of exact modulated signals using ADS Ptolemy and co-simulation with envelope

circuit simulator to establish Power Amplifier Linearity.

Section VIII presents Amplifier Simulation Results and Layout. This section demonstrates measurement results from two design examples.

Section IX draws conclusion that a first pass success can be guaranteed for a power amplifier provided proper design flow is established and a strong co-simulation environment is used.

II. Power Amplifier Performance

Figure 1 shows Radio Frequency Front-end of a typical radio operating in full duplex mode. Figure 2 shows the same for a half duplex radio.

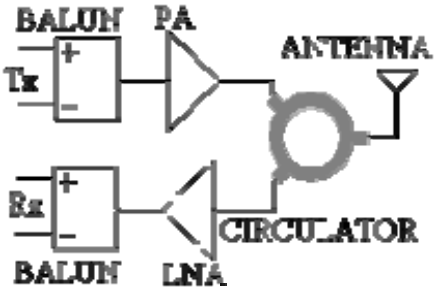

Figure 1: RF Front-end for Full Duplex

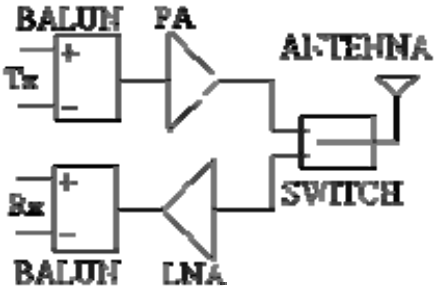

Figure 2: RF Front-end for Half Duplex

Example of a full duplex radio is a mobile phone. Separate frequency bands are allocated for transmit and receive. Such a system is also called Frequency Division Duplex or FDD. Wireless LAN is an example of a Half Duplex radio. Transmit and receive take place in same frequency band. Antenna is switched between transmitter and receiver using Transmit-Receive (T/R) Switch. These two radio topologies place different performance constraints on PA. In former case bandwidth of PA has to be constrained and in later case PA is required to be rugged. Losses in circulator and switch are same.

Small Signal Vs Large Signal

Small Signal refers to the input power to a gain stage such that DC trans-conductance of the active device is the same as its AC trans-conductance. For a BJT, the signal voltage amplitude has to be lower than $V_T\,(KT/q)$ and for an FET, the signal voltage amplitude has to be lower than $2\,V_{OV}$ (overdrive voltage) for small signal performance. Signal voltage levels above these are referred to as large signal.

As the power level goes up the bias point of the device changes and device is said to be RF biased or self biased.

Gain

Ratio of the power at the output (P_{out}) to the power at the input (P_{in}) of a PA is called Gain.

Ratio of the power delivered to the load to the power delivered from the source is called *Power Gain*. Power Gain includes both input and output mismatch losses.

Ratio of the power available at the load under conjugate matching at the output to the power available from the source under conjugate matching at the input is called *Available Gain*.

Ratio of the power available at the load under conjugate matching at the output to

the power delivered by the source is called *Transducer Gain*. Usually Power Gain is specified along with the return losses.

Small Signal Gain and Return Losses are plotted across frequency while Large Signal Gain and Return Losses are plotted across input or output power for center and band edge frequencies. Power Gain is a pure number (P_{out}/P_{in}) and can be expressed in decibel (dB) as

$$\text{Gain}_{dB} = 10\log_{10}(P_{out}/P_{in}) \qquad \text{equ.1}$$

$$\text{Or Gain}_{dB} = P_{out\_dBm} - P_{in\_dBm} \qquad \text{equ.2}$$

Return Losses

Ratio of the power reflected back to the source to the power incident at the input of a PA is called *Input Return Loss*. Same definition holds for small signal as well as large signal. Input match is usually a conjugate match. It moves with input power and Input Return Loss changes with input power.

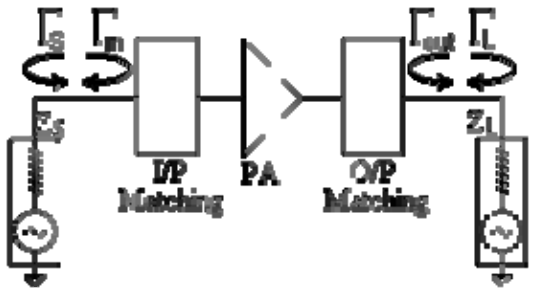

Figure 3: Return Losses for a PA

Power Amplifier is not a bilateral and not a reciprocal network. Output Return Loss is simulated and measured by putting in power at the output port. Ratio of the reflected power to the incident power is called *Output Return Loss*. Output Return Loss is always measured as small signal. It changes as well with the input power. To distinguish between power at the output due to input and reflected power from the output of a PA, slightly offset frequency is used. This we will demonstrate in one of the ADS Harmonic Balance Test Bench.

Return Loss and Gain in terms of Scattering Parameters

Figure 3 shows reflection coefficients at the input and the output of a PA. They are related to small signal scattering parameters (S-Parameters) by the following relations-

$$\Gamma_{in} = V_{in}^{-}/V_{in}^{+} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \qquad \text{equ.3}$$

$$\& \ \Gamma_{out} = V_{out}^{-}/V_{out}^{+} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \qquad \text{equ.4}$$

For conjugate match at the input and the output, $\Gamma_L = \Gamma_S = 0$

$$\Gamma_{in} = S_{11} \ \& \ \Gamma_{out} = S_{22} \qquad \text{equ.5}$$

Input Return Loss in dB is defined as

$$RL_{input} = -20\log(1/\Gamma_{in}) \qquad \text{equ.6}$$

Output Return Loss in dB is defined as

$$RL_{output} = -20\log(1/\Gamma_{out}) \qquad \text{equ.7}$$

Power Gain expressed in terms of S-parameters is given by

$$G_P = \frac{|S_{21}|^2\left(1 - |\Gamma_L^2|\right)}{\left(1 - |\Gamma_{in}^2|\right)\left(1 - S_{22}\Gamma_L\right)} \qquad \text{equ.8}$$

For match to characteristic impedance, $\Gamma_L = \Gamma_S = 0$ and $\Gamma_{in} = \Gamma_{out} = 0$

$$G_P = |S_{21}|^2 \qquad \text{equ.9}$$

Power Gain in dB is given by

$$G_{P\_dB} = 20\log_{10}(S_{21}) \qquad \text{equ.10}$$

And Available Gain is dB is given by

$$G_{Available\_dB} = 20\log_{10}(S_{21}) \qquad \text{equ.11}$$

Input Return Loss and Power Gain are expressed in terms of power or reflection coefficients under large signal condition.

Nature of Gain and Output Power Vs Input Power

As the DC Supply voltage or current may be limited, increasing input power does not increase the output power linearly beyond certain power level. The power gain drops with increase in the input power. This is referred to as Gain Compression. Input RF Power may shift the bias point of the device up boosting the gain just before compression, referred to as Gain Expansion.

Figure 4 shows that the output power increases linearly with the increase in the input power, initially. This region is referred to as linear region. Linear systems require the PA to be operated in this region.

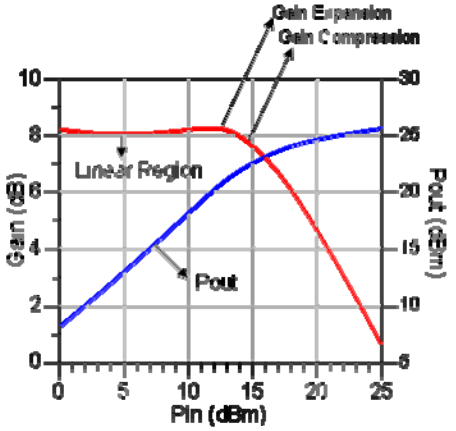

Figure 4: Compression Characteristics of a Gain Stage

As the output power gets limited by the DC Supply Power, it does not increase linearly and demonstrates higher order nature. This is referred to as compression.

Efficiency

In Power Amplifier, DC Power is converted to RF Power at the output. In battery operated devices this conversion has to be efficient. Various ways efficiency of a PA is defined are- Drain or Collector Efficiency and Power Added Efficiency (PAE). Figure 5 shows the nature of PAE Vs Input Power.

$$\text{Drain Efficiency} = \frac{P_{out}}{P_{DC}} * 100 \qquad \text{equ.12}$$

$$\text{PAE} = \frac{P_{out}}{P_{in} + P_{DC}} * 100 \qquad \text{equ.13}$$

Or

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} * 100 \qquad \text{equ.14}$$

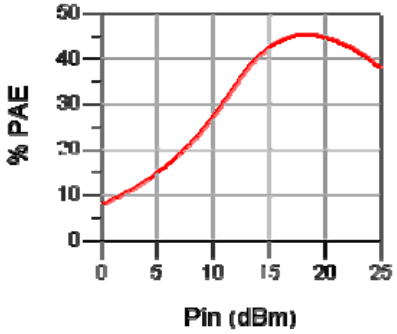

Figure 5: PAE Vs Input Power

Linearity

Non-Linearity results in out-band emissions causing inter channel interference and reception of symbol in error. These two effects are quantified using Adjacent Channel Power Ratio (ACPR) and % Error Vector Magnitude (%EVM) respectively. Figure 6 shows output spectrum from a PA amplifying CCK Modulated Signal.

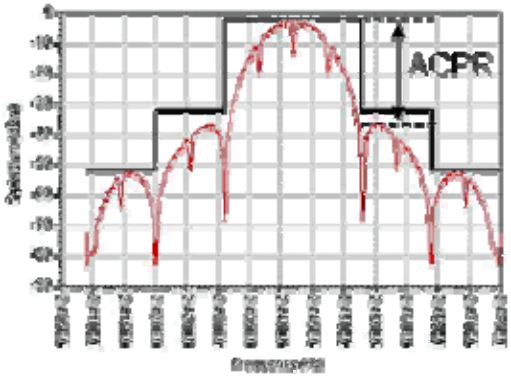

Figure 6: Output Spectrum of WiFi Tx

III. Design Flow for Power Amplifier

Figure 7 shows typical design flow of a PA usually followed in the industry. Slight variations are expected based on PA Topology & IC and Board Manufacturing Technologies involved.

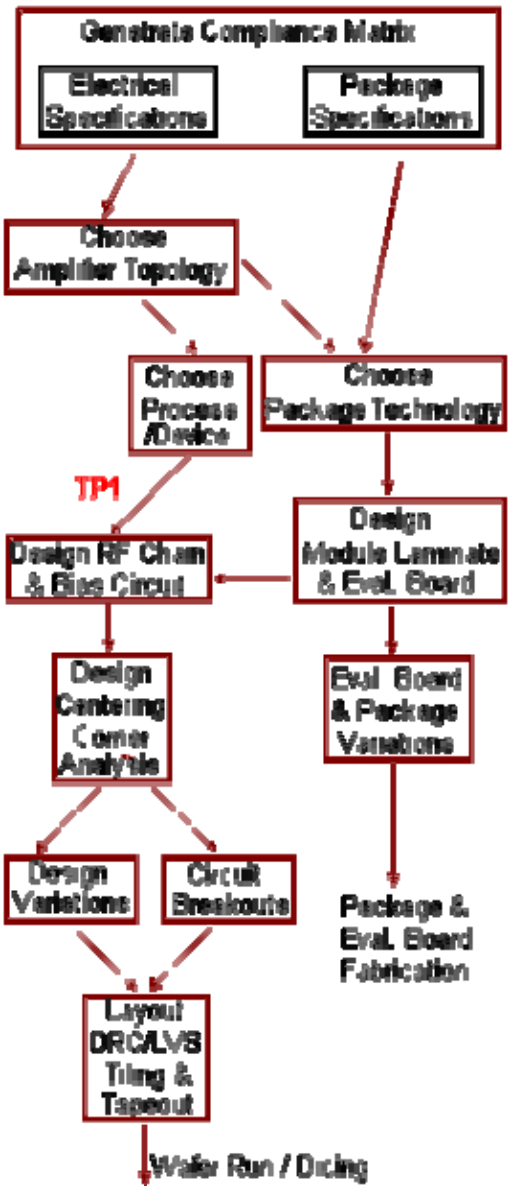

Figure 7: Typical Design Flow of a PA

Design starts with the definition of a compliance matrix. Compliance Matrix lists the desired electrical and physical specifications discussed in section II.

Designer has to choose PA Class based on wireless application. Figure 8 shows various Classes of Power Amplifier.

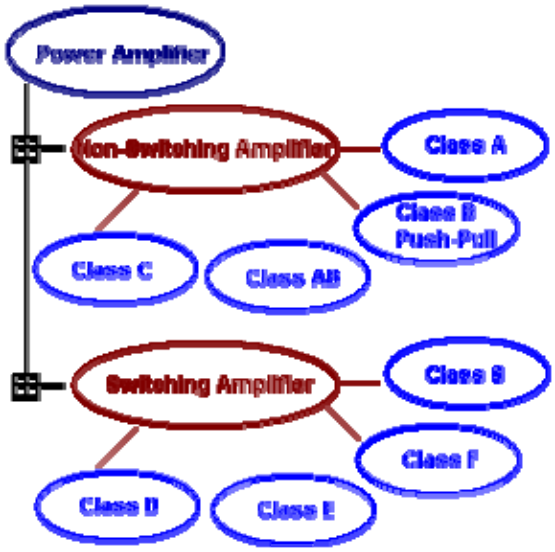

Figure 8: Power Amplifier Classes

Table 1 compares these classes based on Device Utilization Factor, Ideal Highest Efficiency and a typical feature.

Class	DUF	% Eff.	Comments
A	0.125	50	360 ° cond.
B	0.125	78.54	180 ° cond.
C	0.0981	89.6	120 ° cond.
	0.0000	100	0 ° cond.
D	0.318	100	2 pole switching
E	0.0981	100	Opt. Pout at 50% Duty Cycle
F	0.159	100	Load Resonators
S	0.125	100	AC Coup. O/P

Table 1: Power Amplifier Classes

Note* DUF= Optimum Pout/Peak Device Power

For linear power amplification at microwave frequencies, Class AB Amplifiers are used. For constant envelope signals saturated amplifiers are used.

Class C Amplifier is easiest to design but suffers from high harmonic distortion. Class F is best for power amplification due to its best DUF but the merit fades away at high frequencies due to losses in Load Resonators (peaking circuits). Class E is the best for high efficiency power amplification at microwave frequencies but suffers from low DUF. Other amplifier classes are not well known at microwave frequencies.

Once Power Amplifier Class has been identified, a circuit topology is chosen. In case all passive components and bias circuit are fabricated on wafer, a standard Plastic Package or Air Cavity Package can be chosen. In case there are multiple wafers and off-chip passive components a low coefficient of thermal expansion laminate like BT is chosen for module design. Choice of evaluation board laminate is based on cost and performance. Thinner evaluation boards are preferred at high frequencies due to ground via inductance and higher order mode issues at the RF Connectors.

Choice of the process is based on level of integration and device power handling capability. HBT are the best power devices but suffer from high parasitics resulting in narrow band amplifiers. Process with low dielectric metallization stack should be preferred for low loss on-wafer passives.

Figure 7 shows a point TP1 in the design flow. Power Device models are not scalable with device size and suffer from discrepancies due to thermal issues. Compression characteristics depend on layout and package design. Thermal instabilities are not modeled into most of the models. The best way to remove these unknowns in the design is to validate the model by benchmarking same size device. Load pull on the devices can provide valuable information about matching.

RF Chain is designed based on target gain, efficiency, bandwidth, linearity, stability, ruggedness, quiescent current etc. Bias Circuit is design based on noise figure constraints, across supply voltage and temperature corner performance and modes of operation. Figure 9 shows various performance criteria that may affect the design.

Figure 9: Performance Criteria affecting Power Amplifier Design

Once the design is optimized for performance, designer has to follow DOE (Design of Experiment) Method to center design and improve yield. To save design cycle time various sub-circuit breakouts, device breakouts and design variations should be considered for tape-out.

Post layout processing includes performing DRC, LVS, Density Rule Check and Tiling. Tiling may involve adding guard rings around the chip and specifying space for dicing channel.

Prototyping and testing are beyond the scope of this paper. Another important aspect, critical to success of a commercial PA, is automated testing which involves-designing test sockets, developing test sequences etc.

Various steps involved in the design of a power amplifier are listed below-

a) Design Bias De-coupling Circuit
b) Choose proper size of active devices for various stages
c) Bias various gain stages at appropriate bias points
d) Determine individually large signal match for each stage at the input and the output
e) Determine equivalent match for the inter-stage and cascade stages
f) Design on-chip matching circuits
g) Design biasing circuits
h) Add ESD at all critical nodes
i) Layout as per desired board configuration

We will follow this flow for designing power amplifiers presented in this paper.

IV. PA Operation & Design

We will describe operation of a Class E Amplifier and present its design followed by similar treatment for a linear power amplifier.

Figure 10 shows the topology of a Class E Amplifier

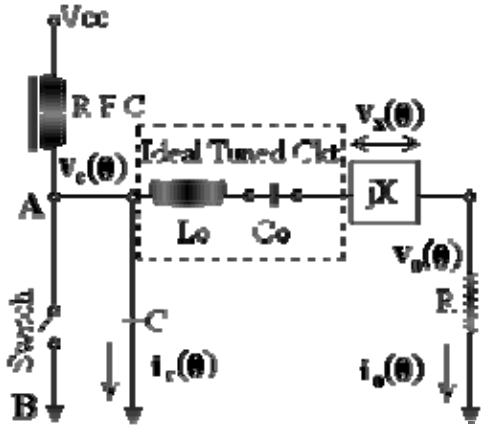

Figure 10: Topology of a Class E PA

Class E power amplifiers are switching amplifiers that operate well into saturation. They have an ideal Drain/Collector Efficiency of 100%. This is achieved by minimizing the loss in the switching device and the loss of the stored energy in the reactive components. In ideal case as shown in Figure 10 the only dissipation of power is in the load resistor.

Principle of Operation of Class-E PA

Ideal Radio Frequency Choke (Bias De-coupling) and a DC Supply act as an ideal dc current source. DC Supply Current is chopped by the switch at switching frequency (f_0). The load network is a series resonant circuit (L_0C_0R) with infinite Q and tuned at f_0. It traps all the voltage harmonics other than the switching frequency and delivers pure sinusoidal voltage across the load R. Switch and Shunt Capacitor (C) trap all the current harmonics and let only sinusoidal current through the load R. Voltage and Current in the load are in phase while in a switch they are in quadrature. Thus dissipation in the device that acts as a switch is ideally zero.

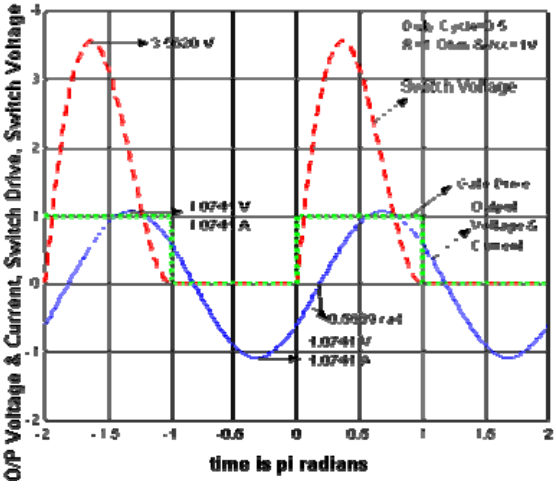

Figure 11: Class E Voltage waveforms

Figure 11 shows switch drive or gate drive that switches the switch on and off. When the gate drive is high switch is off and current flows through the shunt capacitor. Integration of this current gives the voltage across the capacitor, marked as switch voltage. When the gate drive is low the switch is on and current flows through the switch with zero voltage drop across it.

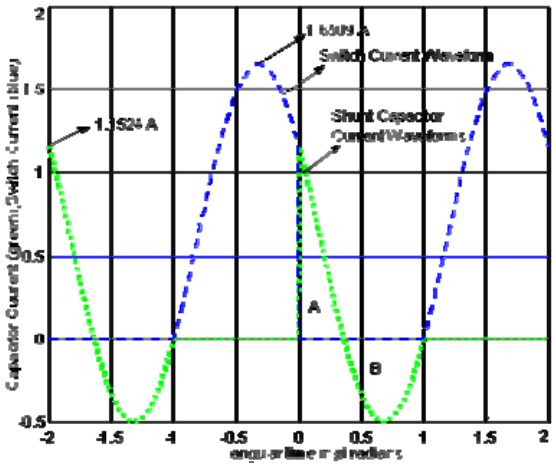

Figure 12: Class E Current Waveforms

Figure 12 shows current waveforms in the switch and the shunt capacitor. The total current flowing through the switch and the shunt capacitor is a DC shifted sine wave as the current flowing into the node A is DC and current flowing into the load is pure sine wave.

Two points are chosen on this DC Shifted Sine Wave for switching the switch on and off such a way that-

a) Area under the current curve (marked A and B) is zero.
b) At switch on the current flowing through the shunt capacitor is zero.

This guarantees that at switch-on the shunt capacitor stores zero energy which could be lost through the switch.

To design such an amplifier, the output has to be tuned not only at the fundamental frequency but also at the harmonics.

Class-E PA Design

The amplifier can be designed using lumped circuit elements as shown in the figure 10. This is based on the assumption of an ideal Class E operation-

a) The voltage across the active device and current through it are in quadrature. This is assured by a switch with zero on time resistance.
b) At switch-on, the energy stored in the shunt capacitor is zero i.e. voltage across the capacitor is zero and current through the capacitor is zero.
c) At switch-off, the current through the switch decays instantly before the voltage across it builds up.

Designing the load network shown in the figure 10 at any load network Q and any Switch-On Duty Cycle (D) requires different analysis.

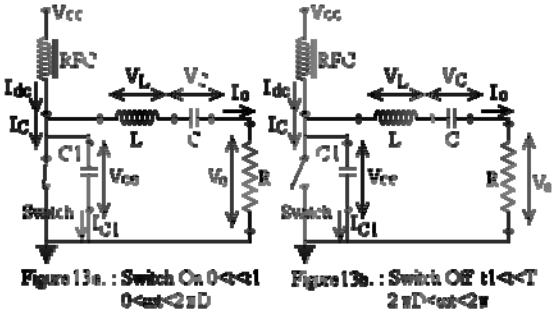

Figure (13 a) and (13 b) show the load network in on and off states respectively. When the switch is on, the shunt capacitor (C1) is shorted and the load resonates at a normalized frequency of $A_1 = f_{01}/f_0$.

When the switch is off, the shunt capacitor (C1) is in series with the series capacitor (C). The load resonates at a slightly higher normalized frequency of $A_2 = f_{02}/f_0$. To design the load network NatTel Microsystems Circuit Designer is used.

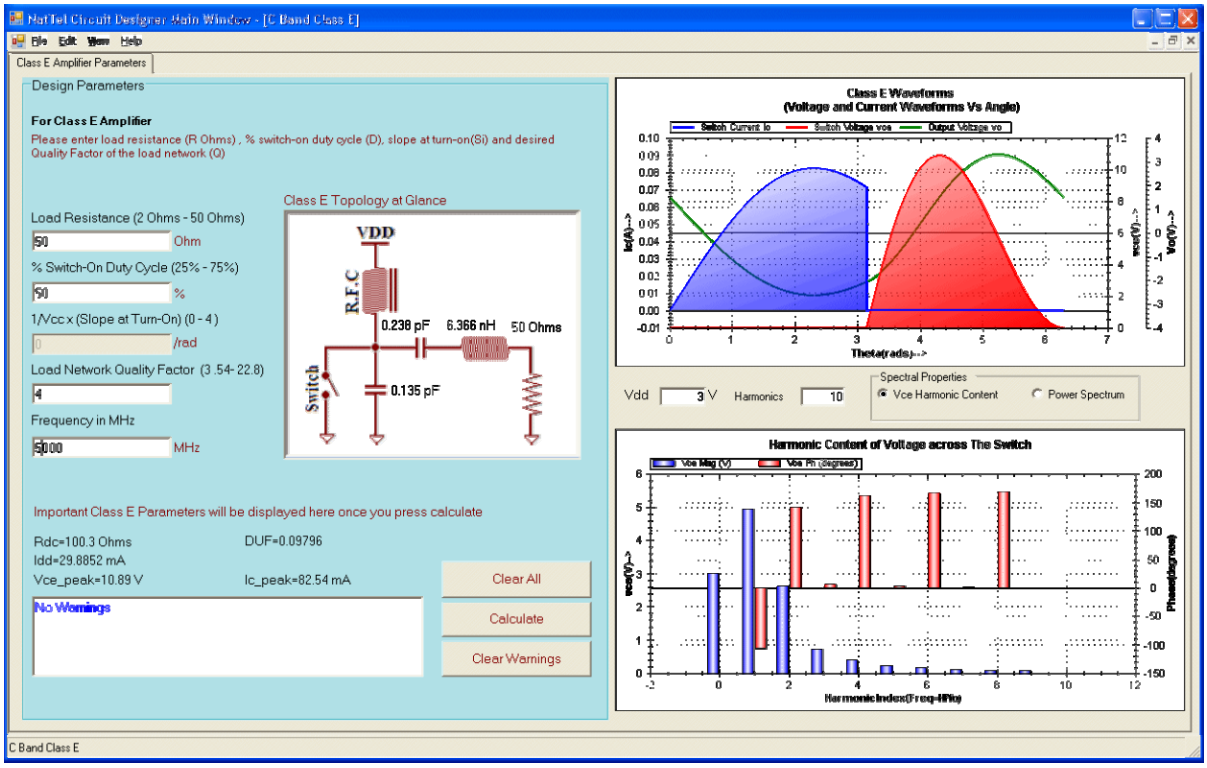

Figure 14: NatTel Microsystems Circuit Designer used to design Class E Load at 5GHz

Figure 14 shows the design of a Class E Amplifier Load with following specifications

Design Specifications	Rating
Load Resistance	50 Ohm
Switch On Duty Cycle	50 %
Voltage Slope at Switch-On	0
Load Network Q	4
Frequency	5 GHz
Supply Voltage	3 V

Table 2: Design Specifications of Class E PA

The output from the circuit designer in figure 14 shows Class E Voltage and Current Waveforms and their harmonic content, the Load Network component values (re-listed in table 3), the DC operating point, Device Stress and Device Utilization.

Load Components	Value
C1	0.135 pf
C	0.238 pf
L	6.366 nH

Table 3: Load Network Component Values

Operating Points	Value
Idc	29.8852 mA
Rdc	100.3 Ohm
DUF	0.09796
Vpeak	10.89 V
Ipeak	82.54 mA

Table 4: Circuit Operating Points

The semiconductor process is chosen based on device stress. The device is sized as per the device stress ratings. Next, we present ADS Simulations of the circuit.

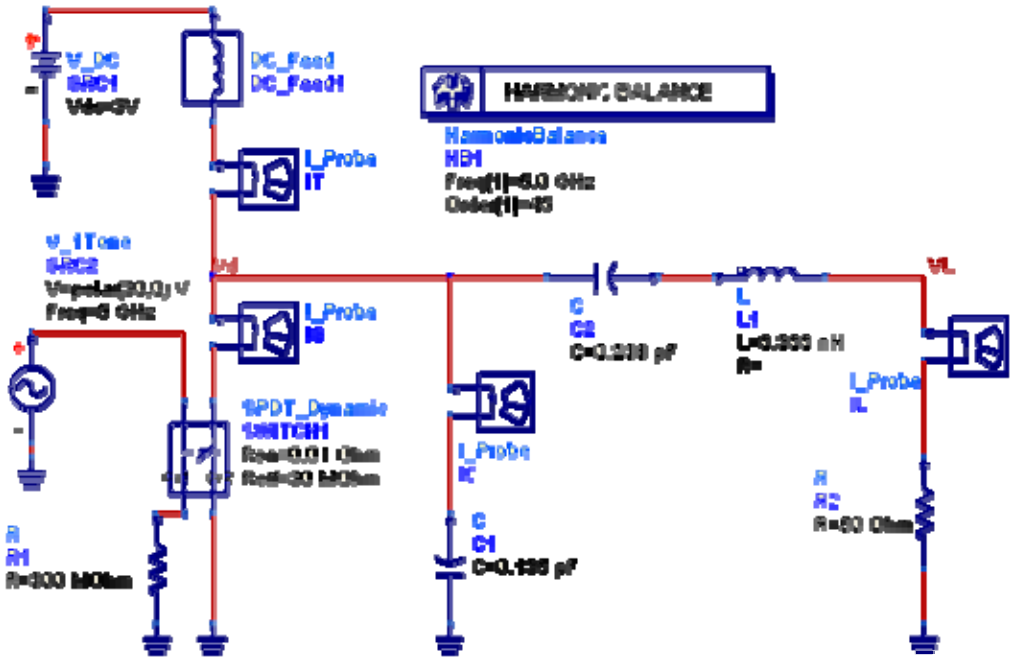

Figure 15: Harmonic Balance Setup for Ideal Class E Simulations

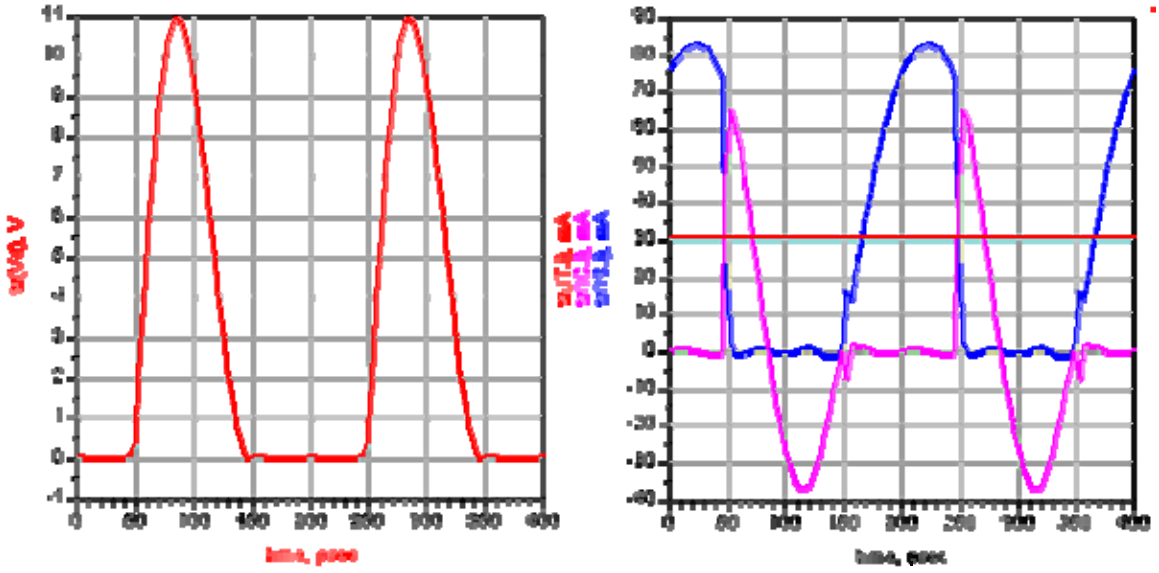

Figure 16: Class E Voltage and Current Waveforms from HB Simulations

Ideal Class E Simulations

Figure 15 shows Harmonic Balance Setup to simulate the designed amplifier. Figure 16 shows the simulated Voltage and Current Waveforms at various nodes in the designed circuit. Near 100% efficiency is achieved. Design strategy from this point will be to replace ideal component with practical ones.

Alternate Class-E PA Design

Thomas B Madder and Zoia Popovic' demonstrated Transmission Line Class E Amplifier Design using microstrip components like λ/4 stubs. Figure 17 shows the Class E Topology.

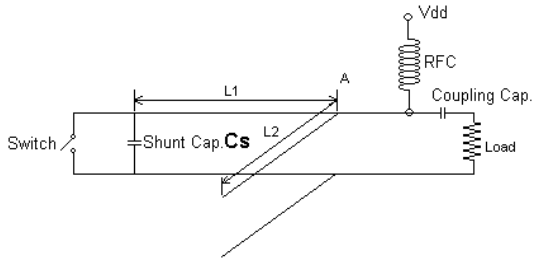

Figure 17: Transmission Line Class E

Fourier expansion of the voltage waveform across the switch shows that harmonic content beyond second harmonic is negligible. This means that load network need not filter third harmonic and beyond components.

The current flowing into the load network, excluding the shunt capacitor, is a pure sine wave. The shunt capacitor (Cs) should be same as that in previous design and should include the output capacitance of the device.

The load network consists of quarter wavelength line and a shunt open circuited stub. This L-section presents open to the device at second harmonic. The ratio of fundamental voltage at the switch to the current gives the desired impedance to be presented to the switch at switching frequency. The L-section is designed to present the desired impedance at the fundamental frequency by altering the widths of the quarter wave sections.

$$Z_{net1} = \frac{V_{s1}}{I_{net1}} = \frac{0.28015}{\omega_s C_s} e^{j49.0524^\circ} \qquad \text{equ.15}$$

Figure 18 shows the complete Class E Amplifier Design for the same specifications except that the load network Q is higher. This is a MIC design on 10 mil thick RT Duroid 5880 Rogers Substrate ($\varepsilon_r = 2.23$). Fujitsu, FLK057WG (W=0.25 mm, L=10um) GaAs MESFET Device is used as a switch.

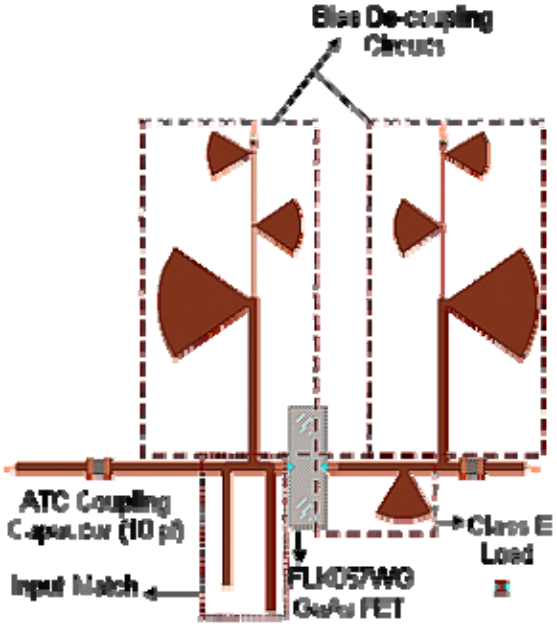

Figure 18: ADS Momentum Layout of 5GHz Class E Power Amplifier

Let us discuss step by step the design of this Class E PA.

Step 1: Design a wideband bias de-coupling circuit (up to third harmonic) using λ/4 long stubs.

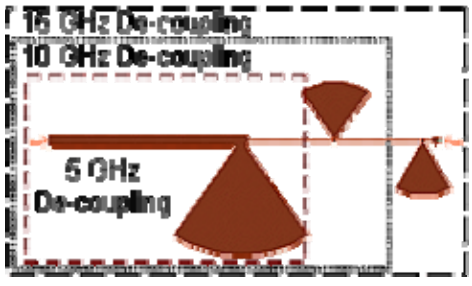

Figure 19: Multi-harmonic de-coupling

Figure 19 shows bias de-coupling network designed to de-couple at 5 GHz, 10 GHz and 15 GHz. Figure 20 shows the decoupling response of the network designed using ADS MOMENTUM and simulated using S-Parameter Circuit Simulator.

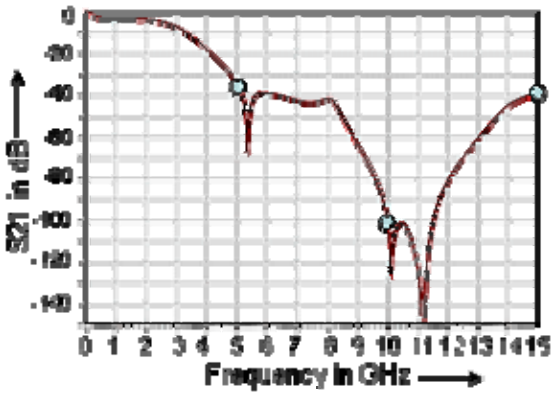

Figure 20: Simulated Response of Bias-Decoupling Circuit

Step 2: Use a switching model of the FET or as in this case fit a switching model using S-Parameters

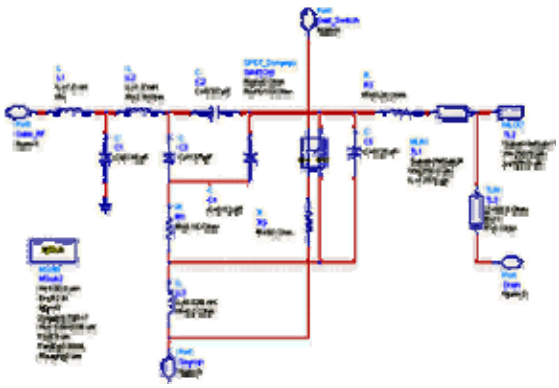

Figure 21: Switching Model of FLK057WG GaAs FET

This model is useful for operating the device is saturation. It is invalid for power back-off. This model is based on parasitics extracted from small signal S-Parameters of the device. Simulations do not present the power sweep for this reason.

Step 3: Design Input Conjugate Match and Load Match.

Load Match consists of λ/4 open circuited radial stub at second harmonic (10 GHz) presenting short to another λ/4 section. The short is transformed to open by this impedance inverter and presented to the switch at second harmonic. Using equ.15 the load impedance is computed as

$$Z_{net1} = \frac{0.28015}{\omega_s C_s} e^{j49.0524^\circ} = 24.35 + j28.06$$

The width and the length of the λ/4 line at the output are adjusted so as to present the computed impedance at the output of the device. As S21 of the device is very low, the input match does not move much with the load.

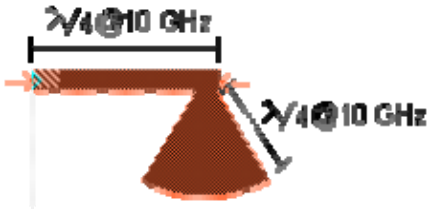

Figure 22: Class E Load Match

A broadband input match is designed using two open circuited stubs as shown in the figure 23.

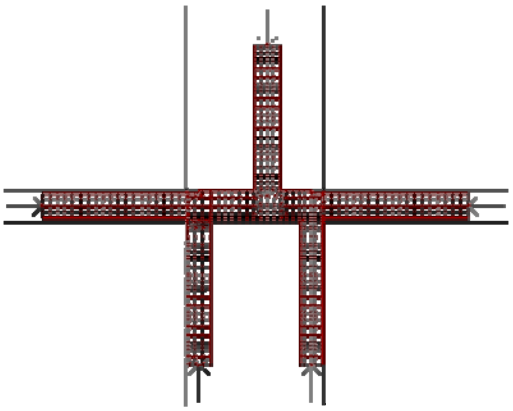

Figure 23: MOMENTUM Layout of the twin stub matching at the input

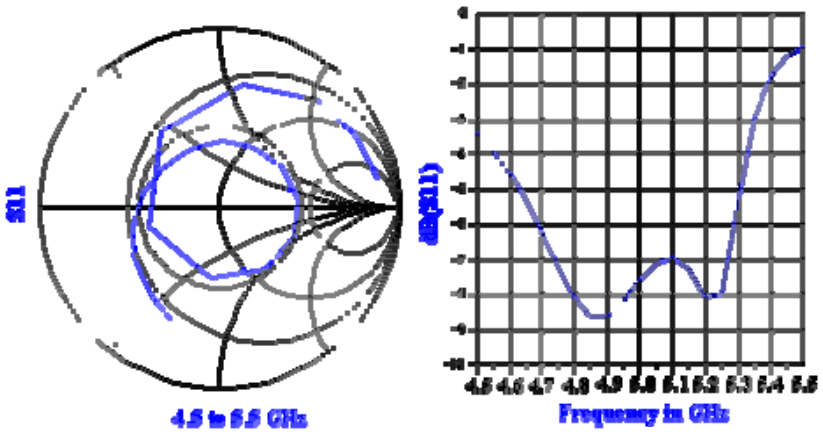

Figure 24: Input Return Loss of Class E PA

Step 4: Model the coupling capacitors as broadband SPICE model.

Figure 24 shows input return loss of the designed power amplifier. Figure 25 shows various simulation setups in ADS.

Step 5: Perform Harmonic Balance and other simulations.

Figure 26 shows simulated response of the designed Class E Power Amplifier. Section VIII presents the measured results.

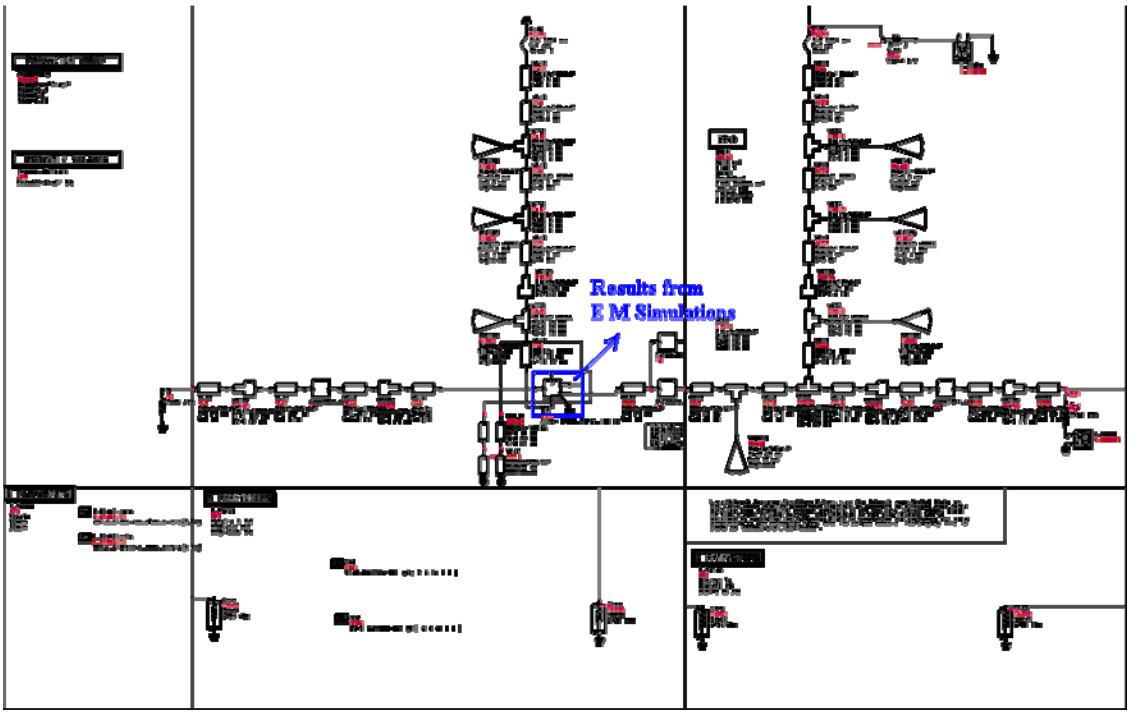

Figure 25: Various Simulations can be performed on same schematic by proper selection of enabled/disabled components and Simulation Controllers

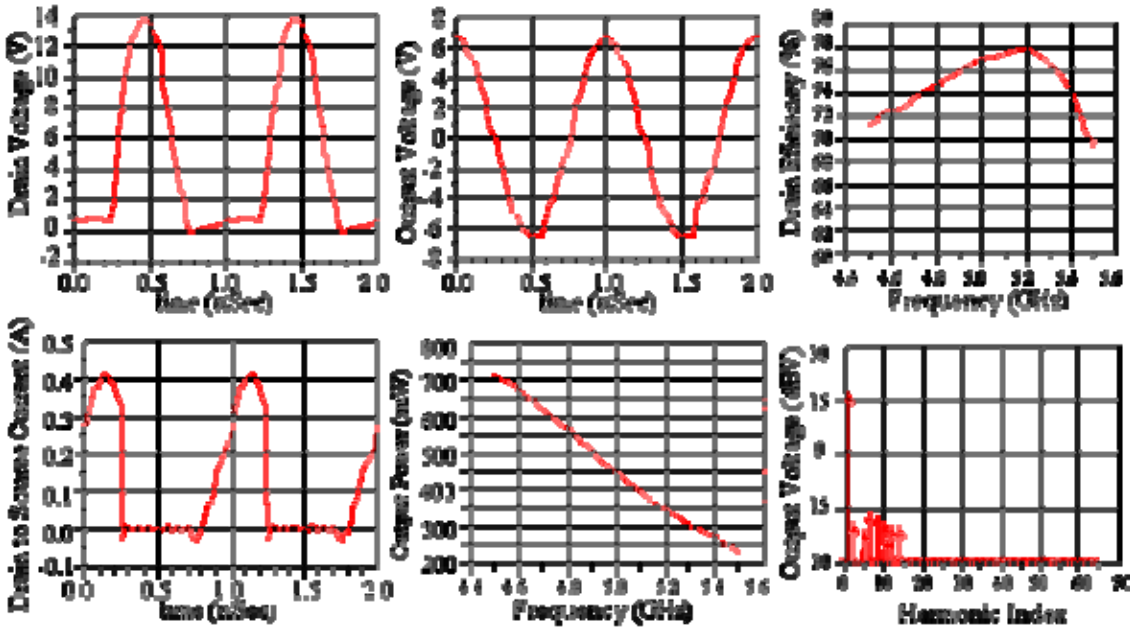

Figure 26: Response of the designed Class-E PA using Harmonic Balance Simulations

Operation and Design of a Linear PA

Linear Power Amplifiers belong to one of the following two categories

a) Cascaded Class AB Power Gain Stages operating at certain backed off input power decided by the Crest Factor of the Modulated Signal.
b) Cascaded Power Gain Stages with some form of linearization- feed-forward, feedback, pre-distortion, or optimization of compression characteristics of various Gain Stages.

In this paper we present a simple three stage MMIC Power Amplifier operating in ISM Band (2.4-2.5 GHz). The design is done in following steps-

Step 1: On-Chip Bias De-coupling Circuit is designed, EM Simulated and Modeled. Section V covers all the techniques required.

Step 2: Each stage is individually designed. We establish a bias point of the stage and demonstrate small signal input/output match ensuring small signal stability. Section VI covers small signal design.

Step 3: We re-tune the power gain stage for optimum compression point by setting up test bench in Harmonic Balance. Section VI covers match optimization and large signal stability.

Step 4: We generate IEEE 802.11 b/g signals using ADS Ptolemy and perform Ptolemy-Circuit Co-simulation. Section VII covers this topic in detail.

Step 5: We comment on sensitive nodes that need to be protected using ESD diodes.

At the end of these steps, we would have a robust design ready for yield optimization.

V. EM design and modeling of passives

In this section we design an on-chip bias de-coupling network using ADS MOMENTUM. Figure 27 shows a parallel resonant LC circuit used for bias de-coupling around center frequency of 2.45 GHz.

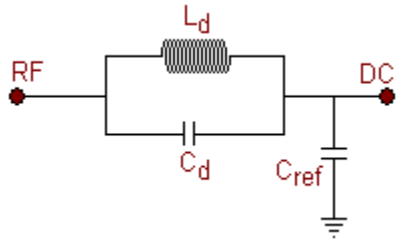

Figure 27: Bias de-coupling circuit

Capacitor (C_{ref}) establishes reference impedance on the DC supply node to be short. Inductor L_d and capacitor C_d anti-resonate at f_0=2.45 GHz.

We choose inductance (L_d) to be 3.6nH. Then the capacitor C_d is given by-

$$C_d = \frac{1}{4\pi^2 f_0^2 L_d} \qquad \text{equ.16}$$

$$C_d = 1.172\text{pf}$$

Capacitor C_{ref}=8pf is sufficient to establish the reference impedance at the DC node to be zero at the center band frequency f_0. The output capacitance of the device appears in parallel with the tank capacitor C_d. Thus C_d has to be lowered by that much capacitance in order to establish high impedance at the drain/collector node.

Figure 28 shows the inductor designed and simulated in ADS MOMENTUM. The dataset file from EM Simulations can be used in the design but may result in convergence issue during frequency domain simulations. Hence we fit a broadband SPICE Model to be used in the simulations. Model has to be valid at least to the third harmonic for proper simulation of compression characteristics.

Proper substrate definition available from the foundry for the process used as well as the board laminate EM Parameters are specified in MOMENTUM Substrate definition. Layout of components complies with grid and layout resolution specifications of the process. DRC Rules are considered during layout.

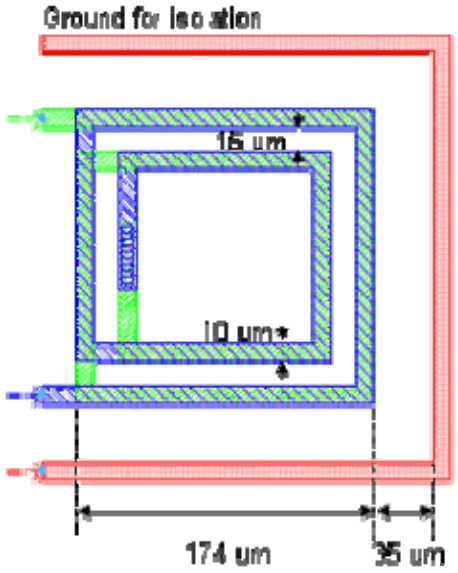

Figure 28: Stacked Inductor Layout (3.6nH)

We simulate the inductor for the frequency range- DC to the third harmonic of the band edge i.e. 7.5 GHz.

Figure 29 shows the SPICE model that needs to be fitted to the S-Parameters obtained from the EM simulation of the inductor.

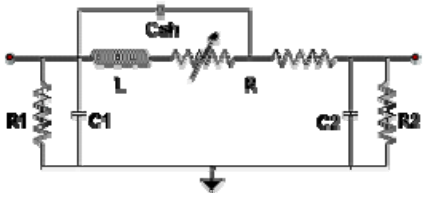

Figure 29: SPICE Model for an inductor

For extracting inductor parasitics we use the following relations-

$$L = \text{imag}(1/-Y12)/(2\pi f_{req}) \quad \text{equ.17}$$

$$R = \text{real}(1/-Y12) \quad \text{equ.18}$$

$$C1 = \text{imag}(Y11+Y12)/(2\pi f_{req}) \quad \text{equ.19}$$

$$C1 = \text{imag}(Y22+Y12)/(2\pi f_{req}) \quad \text{equ.20}$$

$$R1 = \text{abs}(1/\text{real}(Y11+Y12)) \quad \text{equ.21}$$

$$R2 = \text{abs}(1/\text{real}(Y22+Y12)) \quad \text{equ.22}$$

$$C_{shunt} = 1/(4\pi^2 f^2_{anti\_resonant} L[1]) \quad \text{equ.23}$$

We consider series resistance to be quadratic function of the frequency.

We sweep simulation frequency (f_{req}) from DC to 7.5 GHz. Inter-winding Capacitance (C_{shunt}) is determined using the anti-resonant frequency.

Inductance increases with frequency due to lowering skin depth with the frequency. In this model the inductance is assumed constant and Inter-winding capacitance is increased to fit the model parameters. This results in slightly different anti-resonant frequency. As the model is still valid from DC to 7.5 GHz, it can be used in simulations.

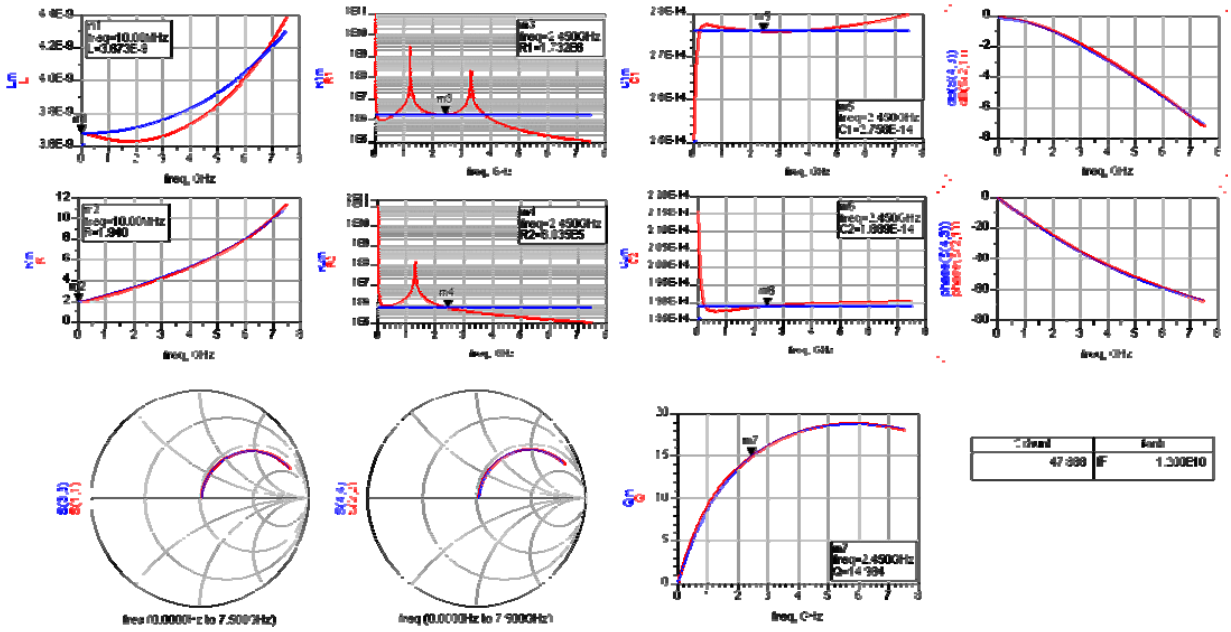

Figure 30: EM Simulated Vs Modeled parameters for the inductor

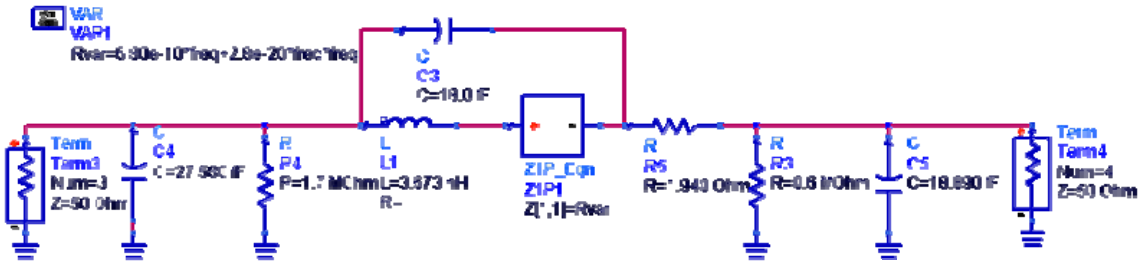

Figure 31: SPICE Model for the Inductor

Figure 30 shows simulated and modeled inductance, series resistance, shunt parasitics and small signal S-parameters. S-parameter simulations show that the model is close to those obtained from EM simulations. Figure 31 shows the fitted SPICE Model for the inductor which can be used in the simulations.

Next we design and model a MIM Capacitor ($C_d = 1.172\text{pf}$) for the bias de-coupling network. Figure 32 shows the layout of the capacitor. Figure 33 shows the SPICE Model for the capacitor that need to be fitted.

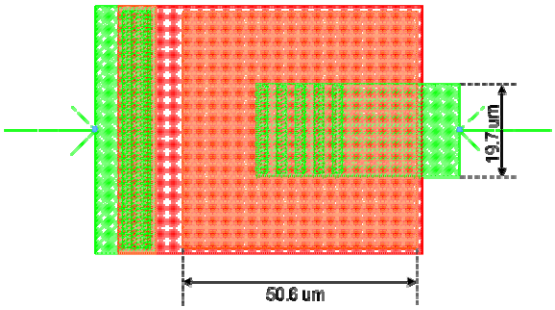

Figure 32: MIM Capacitor Layout (1.17pf)

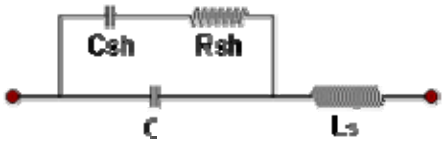

Figure 33: SPICE Model for a Capacitor

For extracting the capacitor parasitics we use the following relationships

$$C = \text{imag}(-Y12)/(2\pi f_{req}) \qquad \text{equ.24}$$

$$R_{sh} = \text{abs}(1/\text{real}(-Y12)) \qquad \text{equ.25}$$

Shunt resistance (R_{sh}) represents the feed-through or leakage between the two terminals. The feed-though component drops with the reducing frequency and is represented by the capacitance (C_{sh}).

$$L_S = 1/(4\pi^2 f^2_{resonant} C) \qquad \text{equ.26}$$

Figure 34 shows EM Simulated Vs Modeled parameters of the MIM Capacitor. Figure 35 shows the fitted SPICE Model for the Capacitor.

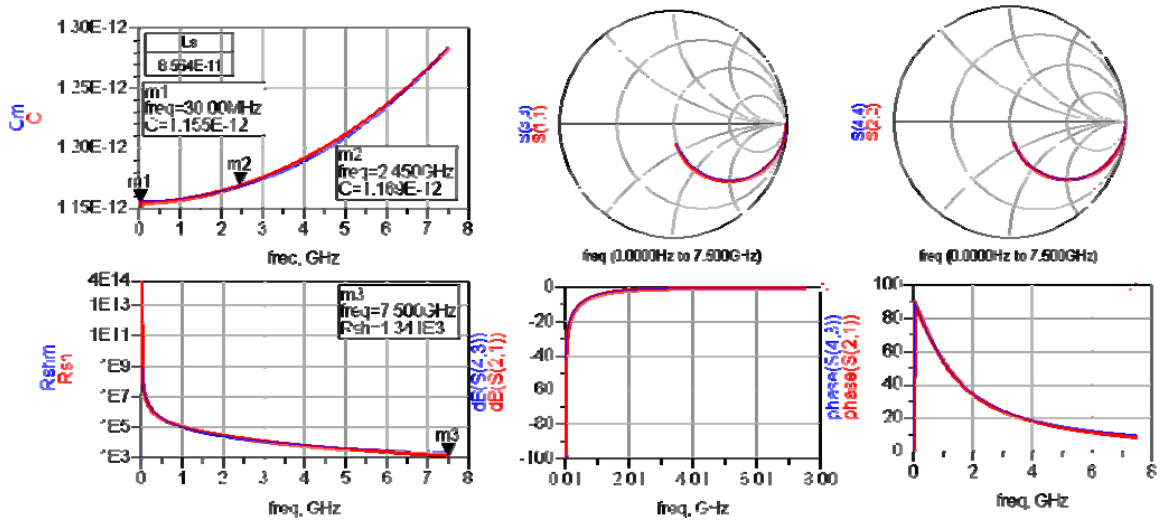

Figure 34: EM Simulated Vs Modeled parameters for the capacitor

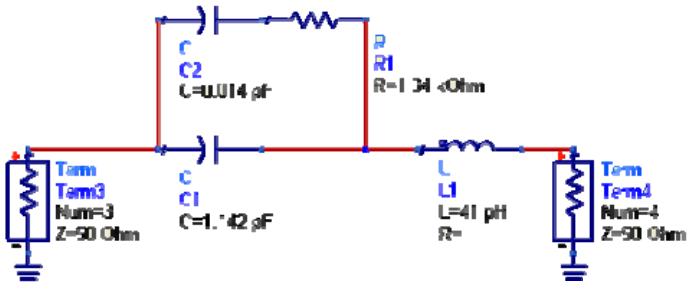

Figure 35: SPICE Model for the Capacitor

Similarly, we can design the by-pass capacitor ($C_{ref} = 8\text{pf}$) and model it. Figure 36 shows the complete bias de-coupling circuit layout. Figure 37 shows the response of the bias de-coupling circuit. The tank capacitor may have to be lowered to adjust the output capacitance of the active device.

Similar design and modeling techniques can be used to design the input and output match of the power gain stages and the inter-stage.

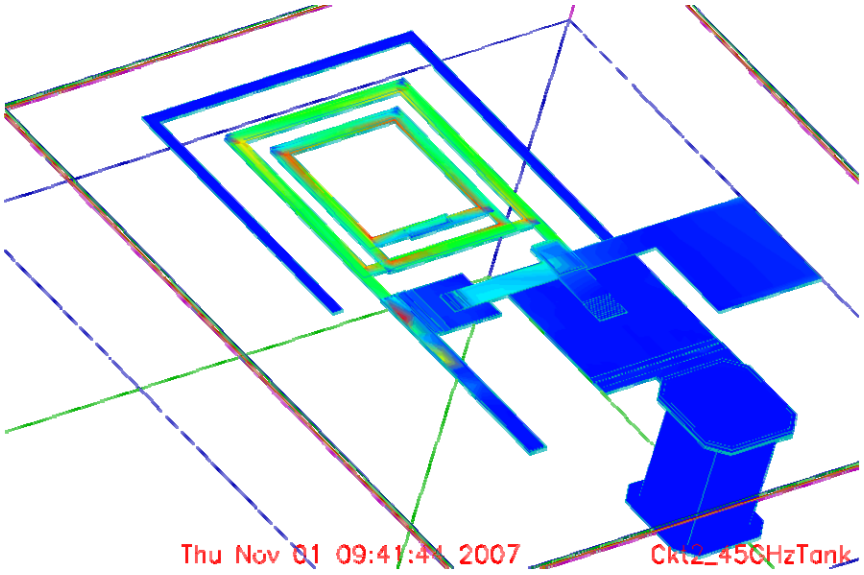

Figure 36: 3D Visualization of Bias De-Coupling Network (Current Plot @ 2.45 GHz)

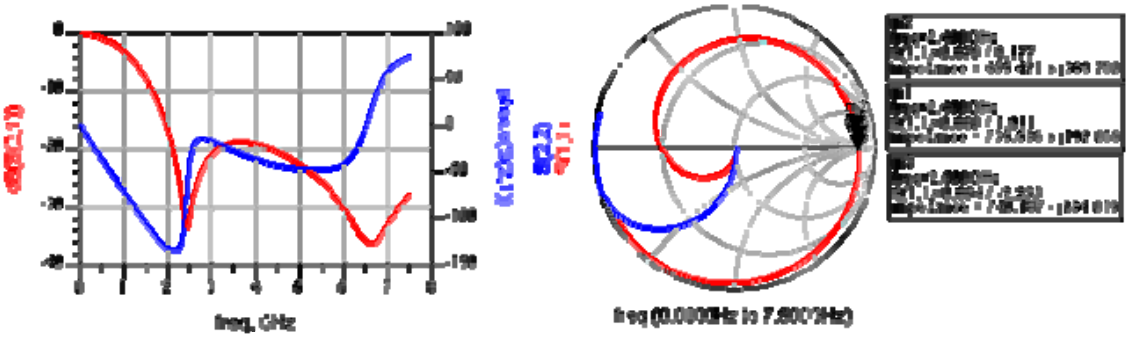

Figure 37: Frequency response of bias de-coupling network

The methodology developed in this section can be used to design and model on-chip passives like inductors and capacitors used to match the power transistors.

Frequency dependence of passives suggests that for broadband and linear systems, EM Simulation is indispensable for IC Design.

VI. Gain Stage Design and Simulations

Using the technique to layout along with the design is vital for first pass success of MMIC PA. There are parasitic extraction tools like DIVA & COLUMBUS RF that let you extract parasitics for a layout, but full field solution is best for coupled parasitics.

In this section, we bias a p-HEMT device with the designed bias de-coupling, match its input and output and simulate its S-Parameters. Figure 38 shows bias point for the power stage of the PA.

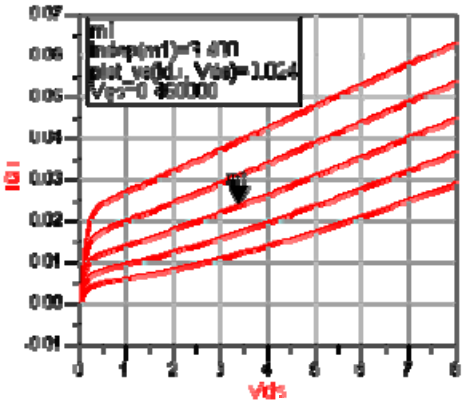

Figure 38: Bias Point of Power Stage (W=1920 um, L=0.5 um)

Figure 39 shows the simulated small signal response of the gain stage. Figure 40 shows S-Parameter Simulation Setup in ADS. High pass matching at input and output of the device assures stability at low frequencies where device gain is high. Lead compensation across Drain and Source provides low frequency stability. High Frequency stability is assured by source degeneration using line and substrate via inductance.

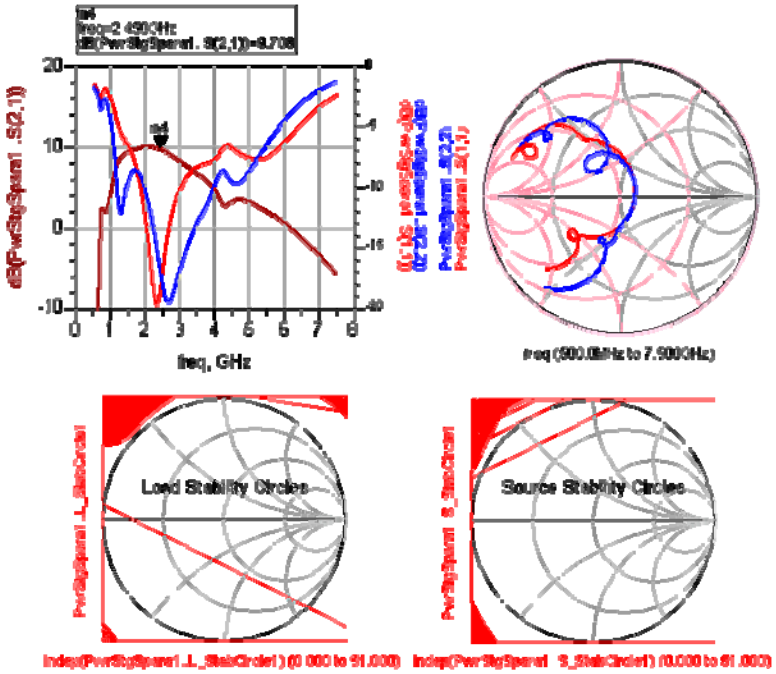

Figure 39: S-parameter response of the power stage

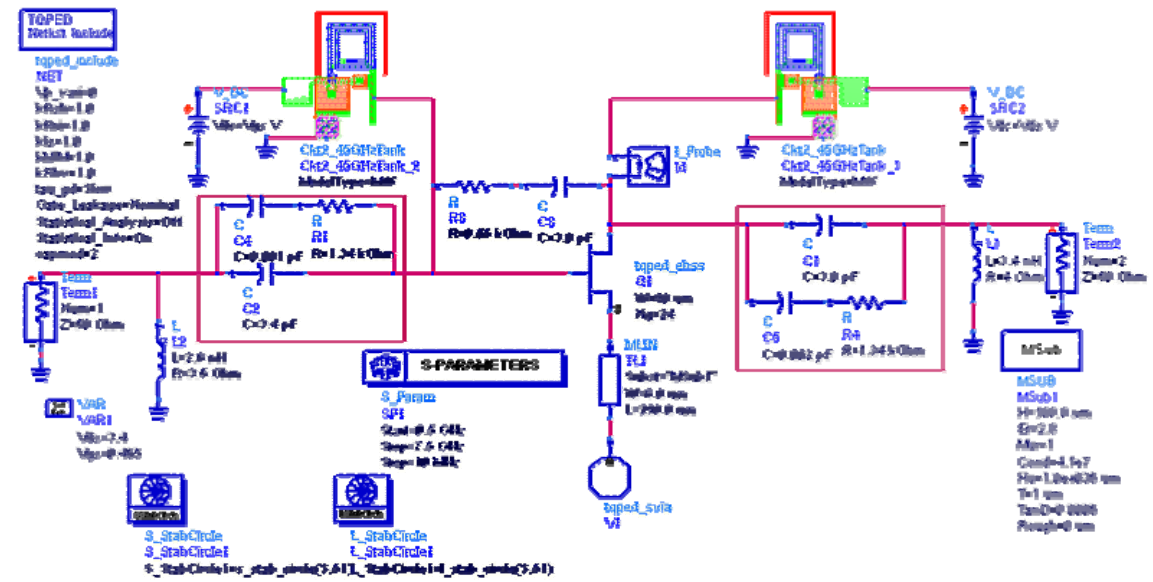

Figure 40: Power Stage small signal match at 2.45 GHz

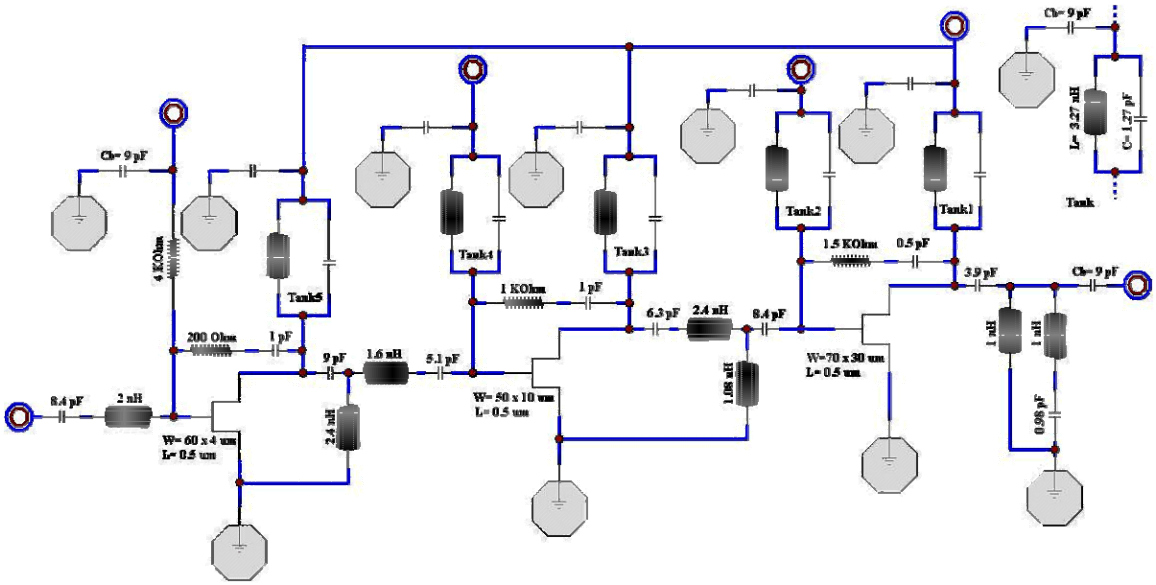

Figure 41: Three Stage Topology of MMIC PA

Impedance matches are separately done for each of the stages. Inter-stage matches are obtained from the transformation of input and output matches of two stages. The design starts with the power stage match, followed by driver stage and pre-driver stage. In match design, the subsequent stages up to the antenna are also included, namely switch and a ceramic band pass filter. All the matches are refined for large signal to adjust the compression characteristics.

Figure 42 shows Harmonic Balance setup to simulate PA compression

characteristics, large signal stability and movement of match with input power.

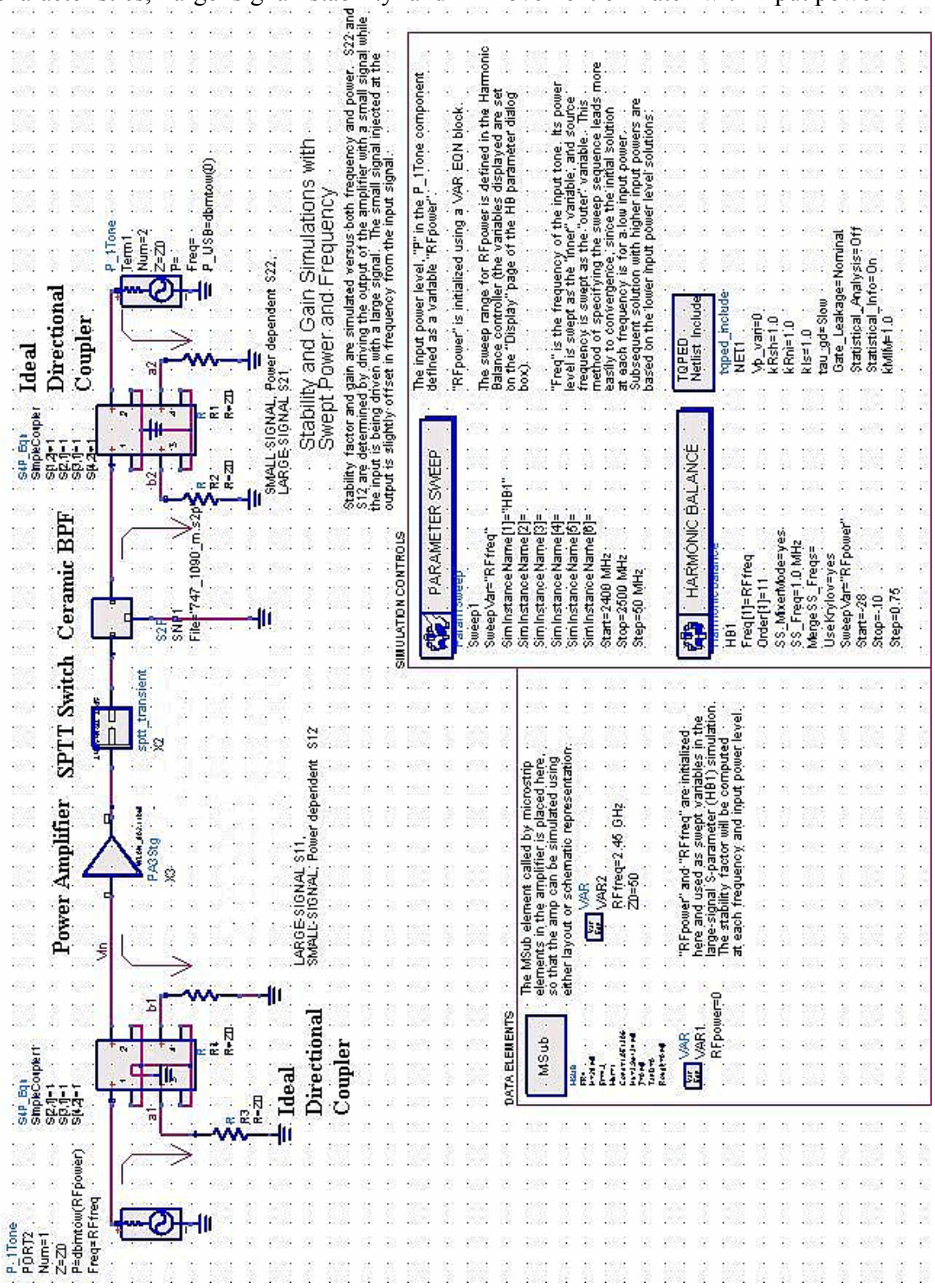

Figure 42: Harmonic Balance Simulation Setup for PA Design

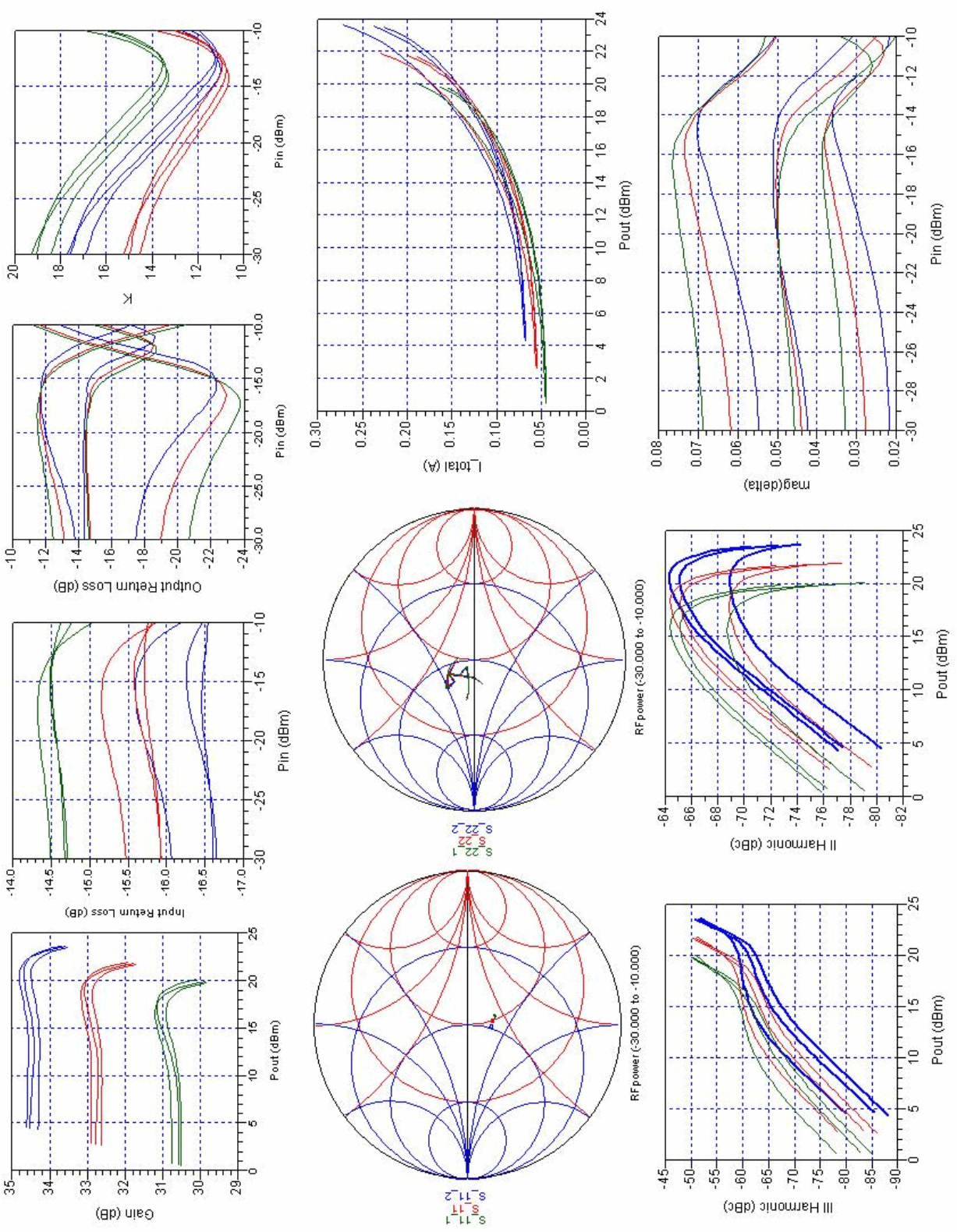

Figure 43: Large Signal Simulations on a three stage PA

Figure 43 shows across power simulation of three-stage PA for three supply voltage (2.9 V, 3.4 V, and 4.5 V) and three frequencies (2.4 GHz, 2.45 GHz and 2.5 GHz).

Figure shows Gain compression characteristics of PA, Input and Output Return Losses, Stability Factor, Input & Output Match movement, Total PA Current, Second Harmonic Power, Third Harmonic Power, and Derivative of Gain Vs the power sweep.

Such a simulation helps in design of the matches of individual gain stages and final multistage PA.

VII. Linearity Simulations using Ptolemy Co-simulation

Agilent ADS provides signal sources for various modulation schemes. The simulation shown in Figure 44 is using a readymade template from Design Examples, used to simulate % EVM and ACPR. The template uses ADS Ptolemy to generate accurate IEEE 802.11 b/g signals for input to a PA. The output is demodulated to predict accurately % EVM and the output spectrum is used to predict ACPR1 and ACPR2. The data rates and modulation schemes can be chosen from a list of options.

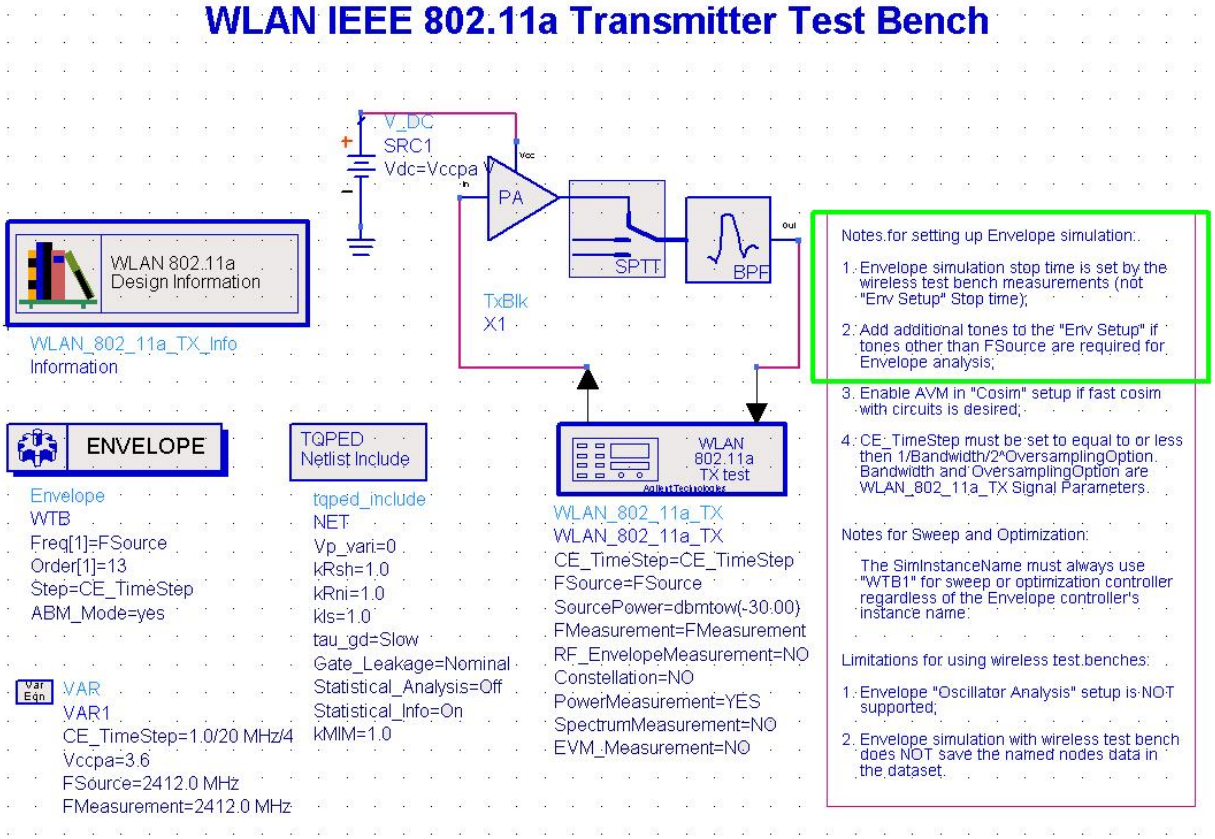

Figure 44a: ADS Bench for % EVM Simulations (IEEE 802.11a, OFDM)

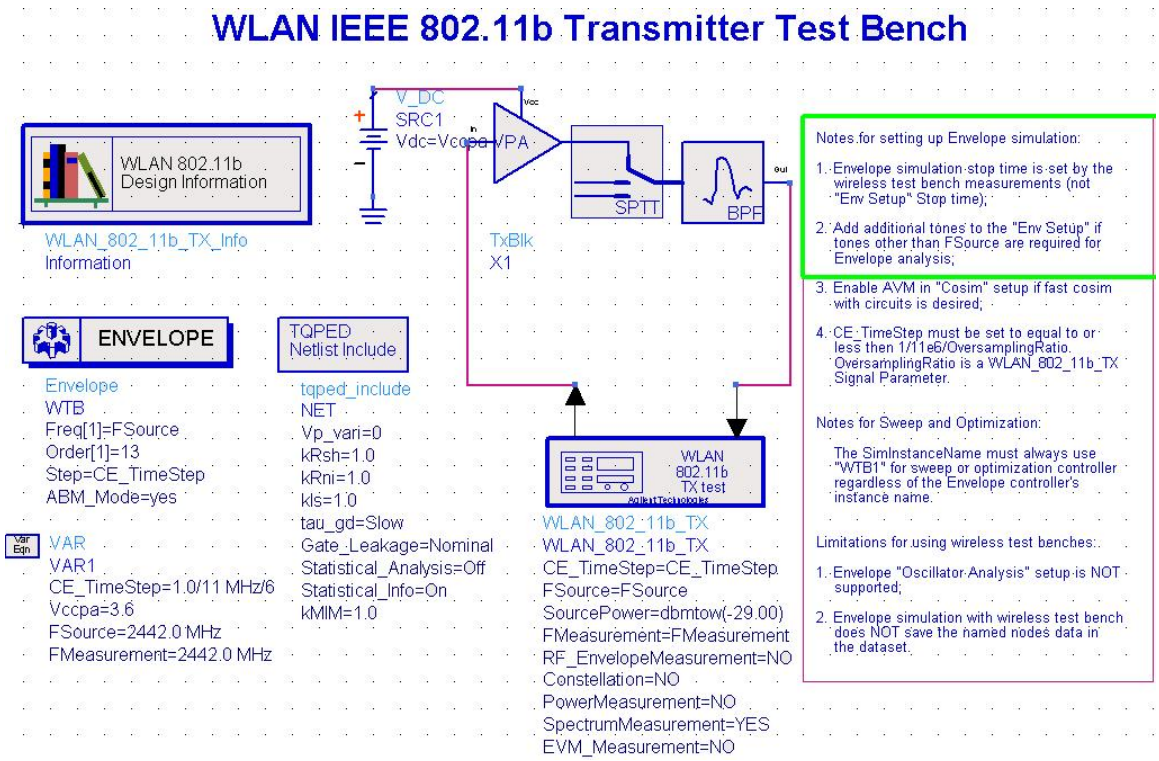

Figure 44b: ADS Bench for ACPR Simulations (IEEE 802.11b, CCK, QPSK)

VIII. Simulation Results, Layout and Measurement Results

Results from linearity simulations for MMIC PA are presented here along with the final Layout. We also present the measured results from the two designs.

Figure 45 shows simulation results under highest data rates or for worst performance. % EVM simulations are carried out for three supply voltages. Figure 46 shows ACPR Simulations. Figure 47 shows peak output power spectrum and the spectral mask for IEEE 802.11 b signal. Figure 48 shows final layout of the three stage power amplifier with on-chip bias circuit and power detector. ESD diodes are added to DC wise floating nodes.

Table 5 and Table 6 list the simulated Vs Measured Results of the two designs.

IX. Conclusion

Both the Power Amplifiers resulted in first pass success without tuning. The paper shows that with proper design flow, modeling and simulations in Agilent Advanced Design System Software a first pass success is possible.

Future Scope for the current work is to include package parasitics in the simulations. We would like to extend the project for design centering, and yield improvement.

Acknowledgements

We would like to thanks LRDE Labs, IISc Microwave Department and Agilent Technologies for all the support.

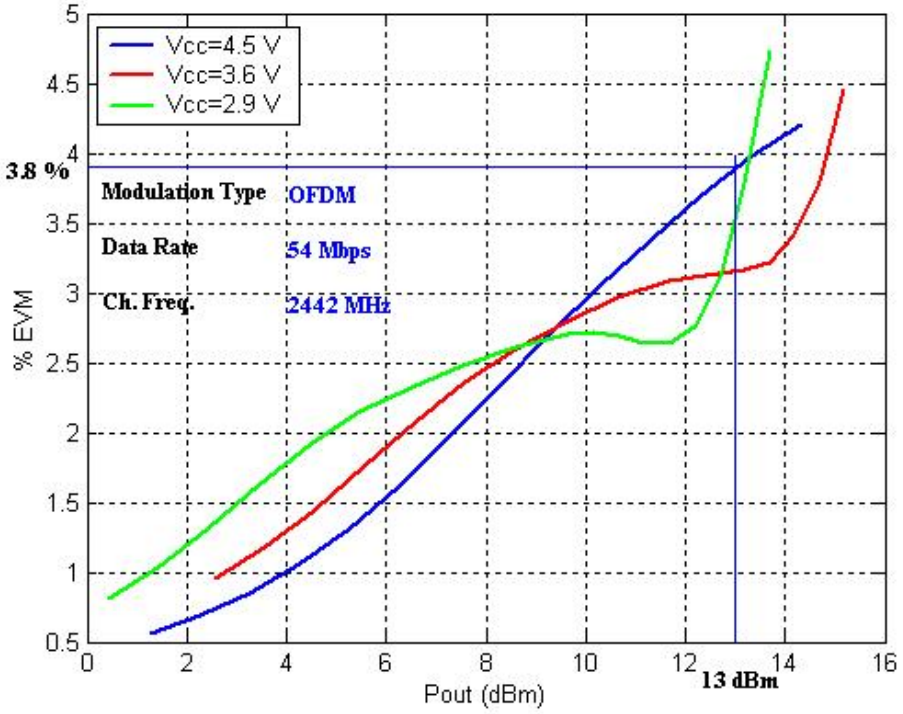

Figure 45: % EVM Simulations for 2.442 GHz Channel

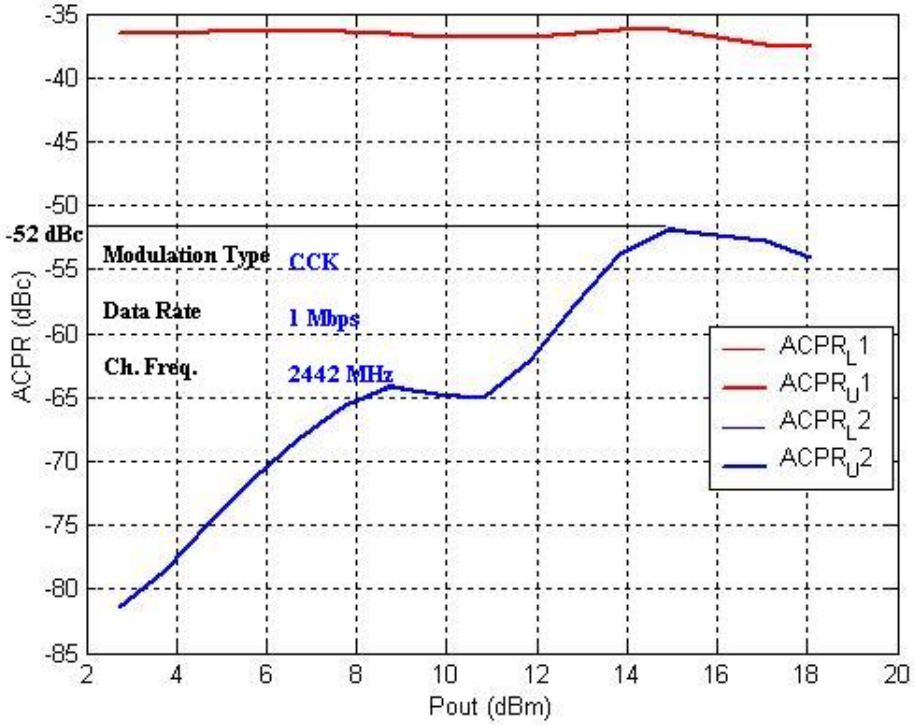

Figure 46: ACPR Simulations for 2.442 GHz Channel

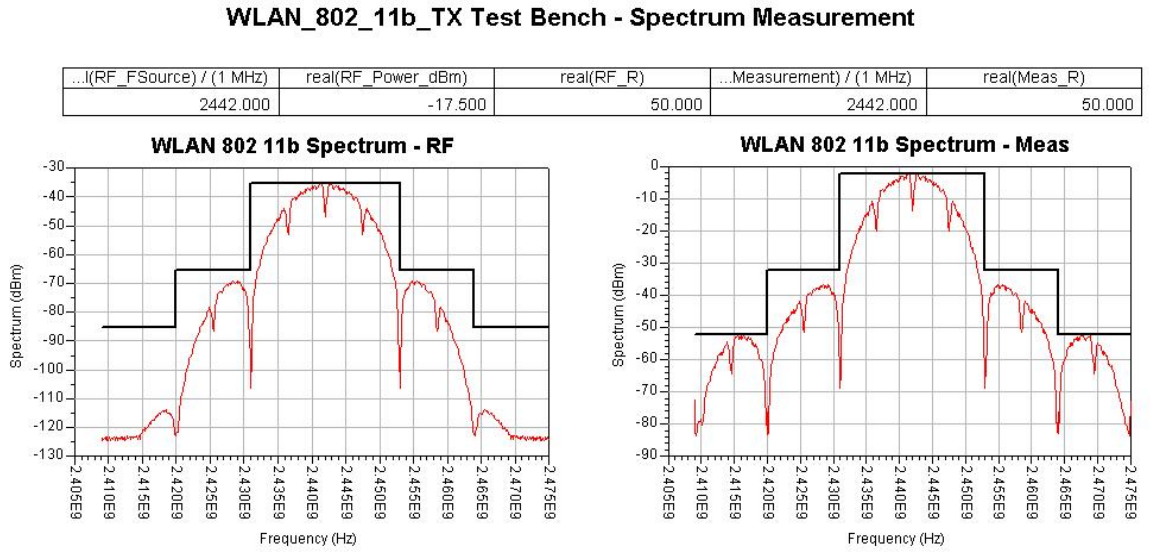

Figure 47: Spectral Performance under peak power

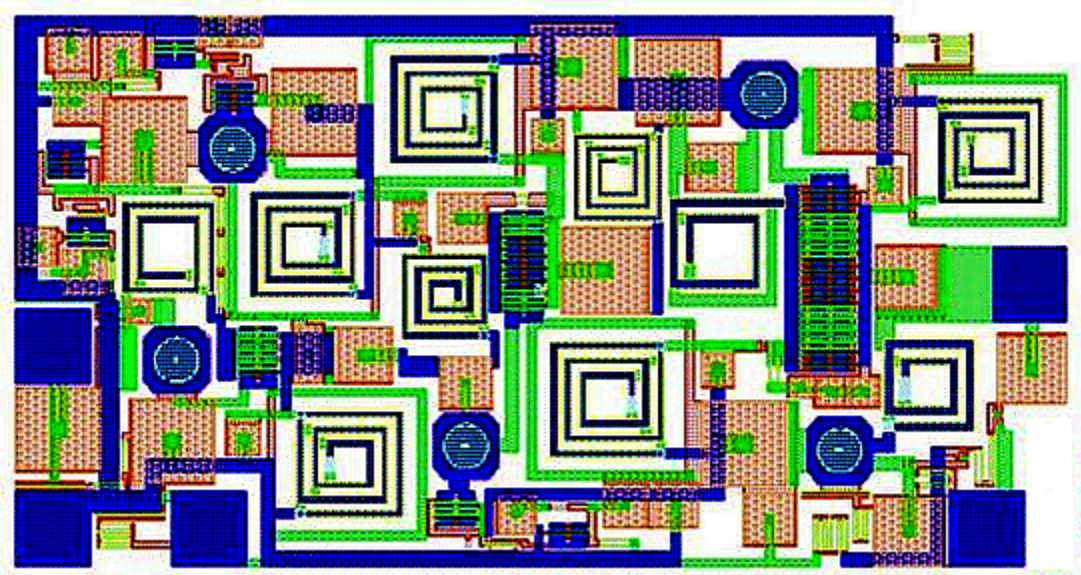

Figure 48: Three Stage MMIC PA Layout in ADS MOMENTUM

	Targeted	Simulated	Measured	Units
Frequency	5	5	5	GHz
Power Out	28	28	27 5	dBm
Gain	10	10	9 5	dB
Input Ret. Loss	<-10	10	7-9	dB
Power Added Efficiency	72	76	68 3	%
Device	FUJITSU WG- Fujitsu MESFET			
Laminate	RT Duroid 5880- Rogers 10 mil thick laminate			

Table 5: Class E Performance

Characteristic Parameters	Unit	Targeted Values	EM Co-Simulated Values	Measured Results
Output Power	dBm	13/16	13/16	13/16
Tx Gain	dB	31.6	30.6/33.6	26
Gain Flatness	dB	2	0.5	0.3
Tx Current	mA	80/110	93/118	100/119
Return Loss (I/P-O/P) (VSWR 2.0:1)	dB	10	12 worse	-14
Stability		10:1	K=16	
Detector Voltage Range		0-1V	0-1V	0-1V
Detector Range	dB	15	15	15
Turn-on/Turn-off		1 us	130 ns/27ns	
ACPR1(b)	dBc	-33	-36	-37
ACPR2(b)	dBc	-53	-52	-54
Harmonics	dBc	-45	-60dBc	

Table 6: Transmitter Performance (Switch and Ceramic Filter included with PA)

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